TRABAJO ESPECIAL DE GRADO

NUEVOS CONCEPTOS Y ESTRUCTURAS DE CONMUTACIÓN IDEAL REALIZAN LA PIERNA DE INVERSOR ALIMENTADA A TENSION CONSTANTE CON MOSFETS.

Presentado ante la Ilustre
Universidad Central de Venezuela
Por el Br. Heyter A. Key A.
Para optar al Título
de Ingeniero Electricista

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CONSTANCIA DE APROBACIÓN

Caracas, 13 de noviembre de 2012

Los abajo firmantes, miembros del Jurado designado por el Consejo de Escuela de Ingeniería Eléctrica, para evaluar el Trabajo Especial de Grado presentado por el Bachiller Heyter A. Key A., titulado:

"NUEVOS CONCEPTOS Y ESTRUCTURAS DE CONMUTACIÓN IDEAL REALIZAN LA PIERNA DE INVERSOR ALIMENTADA A TENSIÓN CONSTANTE CON MOSFETS"

Consideran que el mismo cumple con los requisitos exigidos por el plan de estudios conducente al Título de Ingeniero Electricista en la mención Industrial, y sin que ello signifique que se hacen solidarios con las ideas expuestas por el autor, lo declaran APROBADO.

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Tutor Académico: Profesor Antonino Fratta

Tesis. Torino, Politecnico de Turín, I Facultad de Ingeniería. Departamento de Energía. Año 2012, 72p.

Palabras Claves: Convertidores AC-DC, pierna de inversor, IGBT y Diodo, 2-Mosfet, alta eficiencia, conmutaciones ideales.

Resumen: Basado en las tecnologías actuales utilizadas para la conversión estática de la conmutación forzada, una nueva frontera es definida en el presente estudio. Conmutaciones ideales son realizadas en media potencia y los resultados experimentales obtenidos son reportados mostrando el desempeño y la efectividad.

El "estado del arte" (tecnologías utilizadas en la actualidad) de la pierna de inversor se realiza con IGBTs y diodos Schottky, por sus características eléctricas estáticas y dinámicas. Se propone la pierna de inversor formada por dos Mosfets la cual puede cumplir la función de la referida al estado del arte, que es la bidireccionalidad en corriente y unipolaridad en tensión. Esta nueva pierna de inversor formada por dos componentes idénticos puede ser comparada con la célula fundamental de la conversión estática en los años precedentes, como lo es la célula de conversión formada por dos Tiristores.

Para poder realizar físicamente la pierna de inversor con la tecnología propuesta es necesario conocer las características dinámicas y estáticas de los componentes para poder hacer una gestión correcta de las conmutaciones, y de esta manera se hace la propuesta de un sistema innovativo como lo es el IHC (conmutación forzada ideal, siglas en inglés) que permite realizar conmutaciones en los transistores de forma ideal, esto quiere decir, sin sobretensiones, sin sobre corrientes, sin problemas de compatibilidad electromagnética y con pérdidas reducidas en cada conmutación.

Los resultados experimentales fueron clasificados en cuantitativos y cualitativos para poder determinar la efectividad del sistema realizado, cuyas conclusiones guían a afirmar que la pierna de inversor es posible realizarla para media y alta potencia con mosfets, obteniendo conmutaciones ideales y altísima eficiencia. Una nueva frontera para la conversión está a la vista, teniendo como nuevas prospectivas la realización de la célula fundamental de conversión basada en mosfets.

POLITECNICO DI TORINO

I Faculty of Engineering

Master of Science in Electrical Engineering

THESIS

NEW IDEAL HARD-COMMUTATION CONCEPT AND STRUCTURE REALIZE THE 2-MOSFET V.S. INVERTER LEG

Candidate: Heyter Key Tutor: Prof. Antonino Fratta

October, 2012

To my father's memory and my mother

ACKNOWLEDGMENTS

My first though on the final moment of my career goes to my mother who has being there in every moment to support me and to carry me on when necessary, without a mother like you “mami” be the person that I’m and professional that I’ll be is barely impossible.

From the very first days you take me to school and sais to me “God Bless you, and make you just a good man!”, you planted a seed on me, not only by doing that but in too many other manners; the results of all the love you gave and still give me is this professional who wants to do many things for the woman who gave him more than life.

My father represents a part of me that’s always alive, giving me strength to go forward and never back down in any circumstances, i remember him calling me “Guerrero!” and that’s what i feel i became, a warrior of life. All the love he gave in all the years he was present was more than enough to fill the “love container from a father” to the maximum level and to not get empty anymore.

Then I’ve to thank a girl who is always there for me and loves me in a very strong way, just as i love her, Luz all your support and the things we’ve lived together made my experience through university more than unforgettable, i know so many good things are waiting for us in the future.

Living abroad this two years make realized how important is family and how important are friends in life, so that’s why i have to thank all my friends in Venezuela, always supporting me and believing in me, i have for you all an special place in my heart and my mind, starting from friendsin home who are almost my brothers through all the real friends I’ve done in university.

Special thanks to Professor Fratta who teach me many things included those which i couldn’t ever imagine until now, helping me when necessary to go forward on my final work, and for his particular way to enjoy his work.

To all the people who makes part of this extraordinary journey, people who i help or people who helped me it was a pleasure to found people who teach me with every single experience.

And last but not least I’ll like to thanks UCV (Universidad Central de Venezuela) training me as an Engineer and giving me all the tools to afford any kind of problem I’ll face, because UCV is not only a university is a life trainer.

“God grants victory to constancy” Simón Bolívar

POLITECNICO DI TORINO
Laurea Magistrale in Ingegneria Elettrica
NEW IDEAL HARD COMMUTATION CONCEPT AND STRUCTURE REALIZE THE 2-MOSFET V.S. INVERTER LEG
Candidate: Heyter Key
Tutor: Professor Antonino Fratta

SUMMARY

Abstract: Based on power conversion state of the art, a new hard-switching frontier is defined. The ideal commutation concept is realized in medium-power range. The experimental results are reported, showing performance and effectiveness.

Backgrounds: State of the art canonical cell is realized by two semiconductors, one is a controlled switch while the other must be a diode.

Current semiconductors technologies give a wide range of switches and diodes. For low voltage and low-medium power range, state of the art uses Schottky diodes, on the other hand controlled switches are IGBT.

For very low voltage and low power applications mosfet are used as controlled switches. Particularly for Switched Mode Power Supply the conversion canonical cell is realized by two mosfets, some considerations are taken to control this type of cells.

DC-AC conversion state of the art uses Voltage Supplied Inverter Leg (V.S.I.L.) illustrated in figure a.

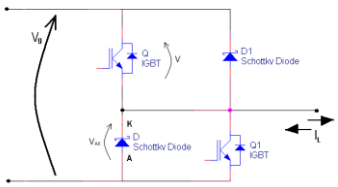


Figure a: State of the art Voltage Supplied Inverter Leg

The simplest V.S.I.L.: is realized by 2-mosfets carrying out all the 4 VSIL functions, as shown in figure b.

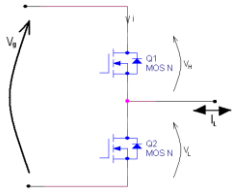


Figure b: The simplest Voltage Supplied Inverter Leg

Over the years, high power static conversion has been realized by two identical components naturally commutated (Current Supplied Inverter Leg), proposed VSIL is the dual cell of the Thyristors one shown in figure c.

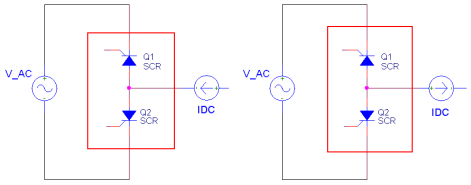


Figure c: First successful canonical cell (CSIL).

Mosfets output capacitance produces EMI problems in commutations if hard-switched. To solve this fact slow down drivers is necessary.

Conduction losses between mosfet and IGBT VSIL are barely equal, advantage can be taken improving commutation losses.

Commutations management: Considering mosfets non linear output capacitance shown in figure d and mosfet body diode reverse recovery which can last around 400ns, a Pulsed Active Desaturation is implemented to control turn-on commutations. Turn-off commutations are controlled by implementing a Snubber and Clamped Circuitry. The whole system is named IHC (Ideal Hard-Commutation) as shown in figure e.

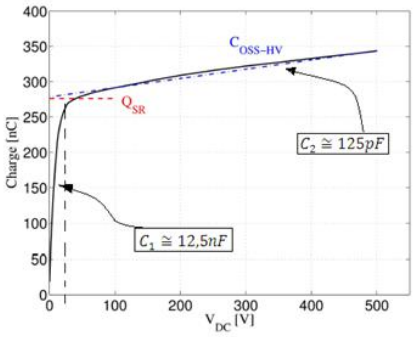


Figure d: Total leg charge for STP42N65M5

IHC is implemented across mosfets drain-source terminal, and is based in two stages by commutation:

Turn-ON (Pulsed Active Desaturations):

*PASR: first stage (few volts), supplies the reverse recovery charge of the mosfet body diode.

*PACR: second stage (tenth volts), supplies the resonance of a circuit inductor with the parasitic capacitance.

Turn-OFF (overvoltage less):

*Snubber and clamped capacitors are preset just after Turn-ON, for next turn-OFF.

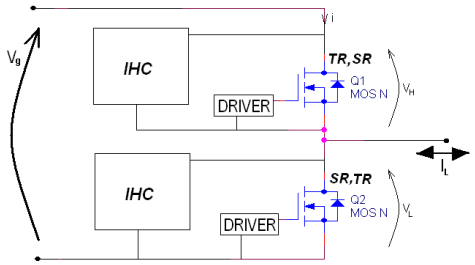


Figure e: VSIL with IHC implemented.

Obtained Waveforms:

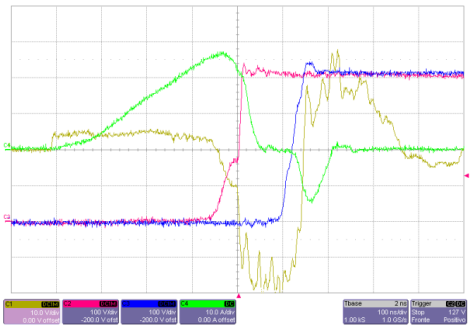


Figure f : Turn-On and turn-off commutation VSIL. (Time scale 100ns/div, voltage scale 100V/div)

Red line represents turn-on commutation, where is possible to distinguish 3 different phases:

1) PASR circuit supplies for approx. 350ns storage charge of the mosfet body diode (5 volts applied)
2) PACR circuit applies 65V through a 500nH inductance, starting the resonance increasing voltage nearby half of DC-link voltage
3) The Mosfet driver senses $^{dv}/_{dt}$ and commands the turn-on; the residual voltage is hard-switched with negligible commutation losses.

Blue line represents a turn-off commutation:

2) Presence of snubber starts from commutation beginning, showing a controlled slope all along.
1) In the last 30V of commutation, clamped condenser start to operate limiting overvoltage and damping the waveform.

Commutation losses: experimental results were obtained and are reported in fig.g for a single VSIL.

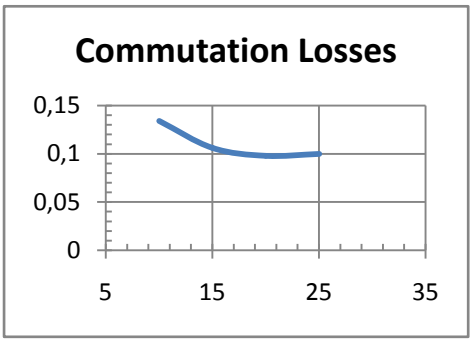


Figure g: Commutation losses [W*100/VA] vs. Switched current [A]; $V_g = 400V$; $f_{SW} = 30\ kHz$

Test bench: in order measure such a low commutation power losses a special instrument was realized to measure conduction resistance, total losses are calculated by measure voltage supplier consumption. Test set-up is shown in figure h.

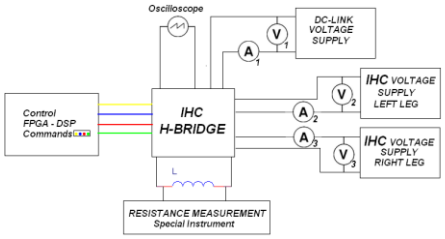


Figure h: Test set-up functional diagram

Conclusions: Experimental results indicates that 2-mosfet inverter leg commutate with ideal commutation waveforms, controlled voltage slope (full compatible), hard-switched turn-on done with almost half of the DC-link voltage (quasi-lossless), turn-off voltage controlled slope (full compatible) final part of the commutation assisted by clamped capacitor (overvoltage less).

A highly efficient inverter leg is obtained as shown in figure g.

A new frontier for the static conversion is shown, introducing a new inverter leg based in two identical components that will define the future for high voltage power electronics.

GENERAL INDEX

LIST OF TABLES

LIST OF FIGURES

INTRODUCTION

Static conversion state of the art for low voltage applications in medium-power will be review in order to highlight current technologies, structures and performance. Over the years technology has changed and continues to change not only in terms of materials but also constructively, leading to a more efficient components and more efficient systems.

More efficient and faster components actually available for low voltage as power mosfet are not used in static DC-AC conversion motivated by them highly dynamic behaviour, representing not a technological barrier but a know-how barrier, because its dynamic and static characteristics should be exploited and actually isn't possible. Actually IGBT are the switching component on Inverter legs which are characterized by its slow turn-OFF dynamic, while SiC Schottky diodes are the complementary semiconductor, chosen by the storageless behaviour on reverse recovery.

DC-DC conversion state of the art for very-low voltage and low voltage applications can be based in different canonical cells motivated by the non linear phenomena and its order of magnitude difference. For very low voltage application high dynamics can be converted into energy saving, while for low voltage became into EMI problems.

Historically one canonical cell has been successful allowing engineers to solve conversion problems, is the Current Supply Inverter Leg realized by two identical components as Thyristors. A new frontier can be proposed for the next future static conversion with a totally dual leg as can be a Voltage Supply Inverter Leg realized by two identical components as Power Mosfet allowing to reduce the number of components for the state of the art inverter leg, with the prospective of impacting not only costs but also physical assembly for the next future of high power static conversion.

For the 2-mosfet leg non linear behaviours dominates the structure in turn-on commutation because mosfet body diode dynamically is very slow when used as Synchronous Rectifier, a large storage phenomenon takes place which implies large current on complementary mosfet and not only this leads to a highly turn-on commutation. On the other hand, turn-OFF commutations are realized with natural dynamic and should be controlled only when large currents must be switched to avoid EMI and overvoltage problems.

Design considerations has to be taken in order to make compatible the proposed leg exploiting its highly dynamical behaviour, but the present study goes further, energetic improvements has been reached by proposing a structure

capable to reduce all the undesired phenomena presents in hard-switching commutation as can be: overvoltage, overcurrent, EMI and commutation losses, making possible ideal commutations and realizing an Inverter Leg that can make a difference for the static conversion next future.

CHAPTER I

STATE OF THE ART AND A NEW FRONTIER

1.1 STATE OF THE ART CANONICAL CELL THEORY

Initially canonical cell can be considered a TRIPOLE CURRENT SWITCH, used in the DC-DC static conversion where the cell is connected with two of its poles to a DC generator (V_g) and connected to the load with the third one, in order to deliver DC current to the load (I_L) while the average value is controlled varying the duty cycle of the cell. Changing the state of the cell is possible to control the current average value, in one position the currents flows from the generator to the load, switching the current deviator will just have a close loop to recirculate.

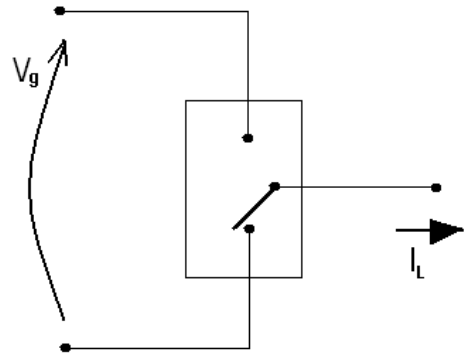


Figure Nº 1: Canonical Cell as a Tripole Current Switch.

To operate as particularly specified before different techniques can be adopted using controlled semiconductors, taking into account that current exchange has to be perfect (deviator objective) willing a constant load current, both semiconductors must work in complement when one of them is open (no current conduction) the other one must be close (current conduction) supporting the load current.

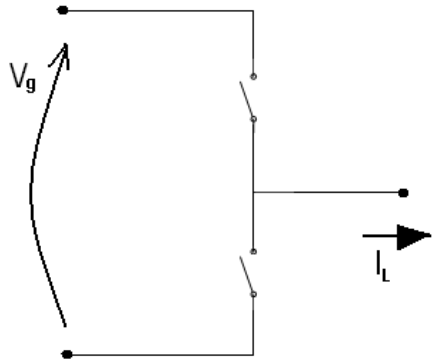


Figure Nº 2: Canonical Cell done with controlled semiconductors.

The static conversion state of the art uses two different semiconductors to make this possible, the first one with a controlled switch while the other one does commutate naturally, in other words uses a Controlled Switch and a Diode.

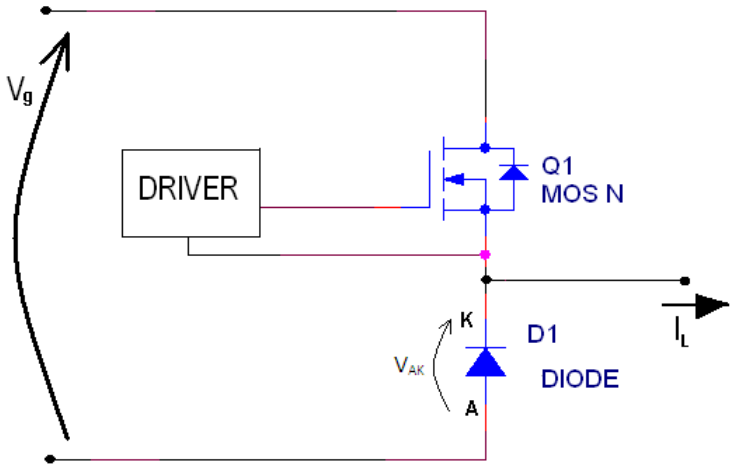


Figure Nº 3: State of the art canonical cell.

In figure 3 is reported state of the art canonical cell formed by a Mosfet (Metal Oxide Semiconductor Field-Effect Transistor) and a diode as example, but is important to know that controlled switch can be an IGBT (Insulated-Gate Bipolar Transistor), a BJT (Bipolar Junction Transistor) or a Mosfet as reported just to illustrate one of the cases.

According to this components disposition the current exchange is realized effectively, when the controlled semiconductor is commanded to be in its ON-state conducting the load current (I_L) naturally the diode goes to its OFF state caused by the Anode-Cathode voltage (V_{AK}) that polarize it inversely, in analogy for the next commutation when controlled semiconductor is commanded to be OFF the diode goes in its conduction state automatically holding through its terminal the conduction threshold voltage (V_{AK}) (in first approximation).

Also is important to note that driver allows the controlled switch to be commanded ON or OFF.

Overall, the tripole current switch is done with two structurally compatible semiconductors, where both electrical characteristics are functionally complementary. The principal caracteristic of canonical cell due to its technological construction is the one quadrant functionality into Current-Voltage plane, then current will only be conducted in one direction (deviation point) while the supply voltage determined by the DC-link in the other two poles, this means the canonical cell will work with unidirectional output current and unipolar input voltage.

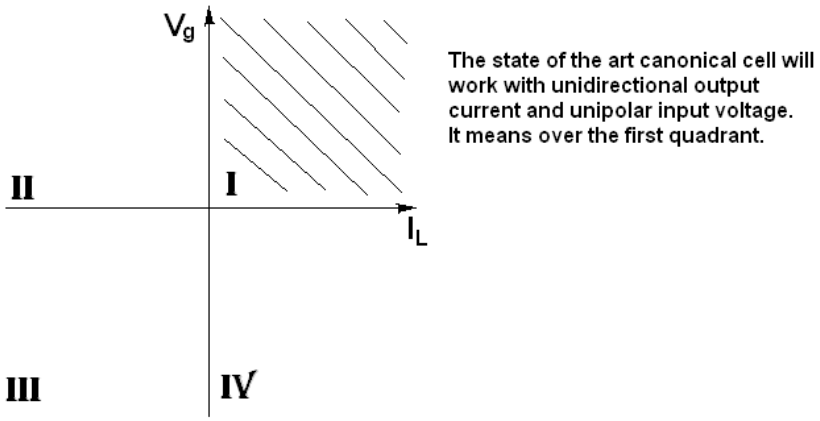


Figure Nº 4: Canonical cell functional quadrant.

In the analysis done until now is specified that load and generator should be connected in specific terminals of the tripole but this is not necessarily a constraint, because from the point of view of the canonical cell load will be connected not in the deviation point but in the other two poles, and vice versa. This implies that will be the external circuit to fix the canonical cell current and voltage values.

1.1.1 Safe Operating Area (SOA)

Just as written before, the work conditions (voltage and current) of the canonical cell will be determined by the external circuit, the response of the cell to the external stimulus are determined by the used switch and diode electrical characteristic. The following analysis is based on the simplest functionality of the cell, without considering subsequent problems.

First of all is necessary to know the single characteristics as follows:

Diode general characteristics:

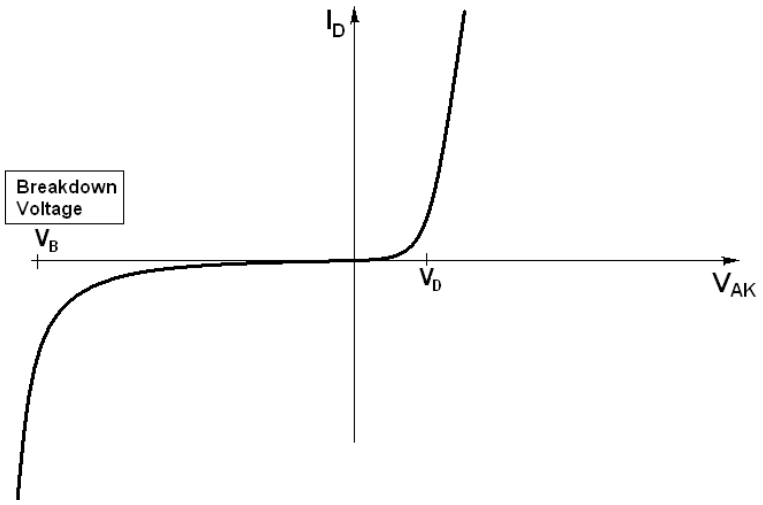


Figure Nº 5: Diode electrical characteristics.

Switch general characteristics:

Typically the switch electrical characteristics are determined by the conducted current and also by the control variable (in the IGBT and MOSFET will be the Gate-Emitter and Gate-Source voltage respectively, for the BJT will be the Base-Emitter voltage), but in the static conversion switches are used in two states, open and close (OFF and ON), each one can be illustrated with as shows in figure 4.

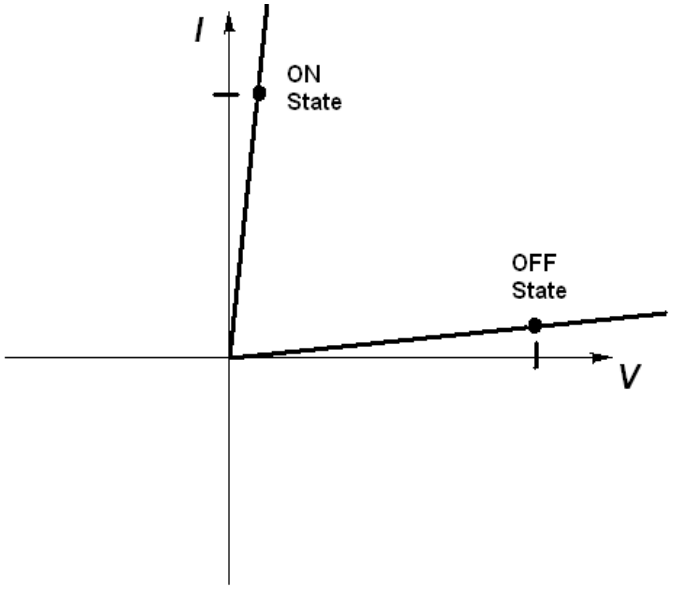


Figure Nº 6: Switch electrical characteristic.

Canonical cell electrical characteristics will be known putting together both electrical characteristics (switch and diode) as follows, considering the complementary functionality between the switch and the diode.

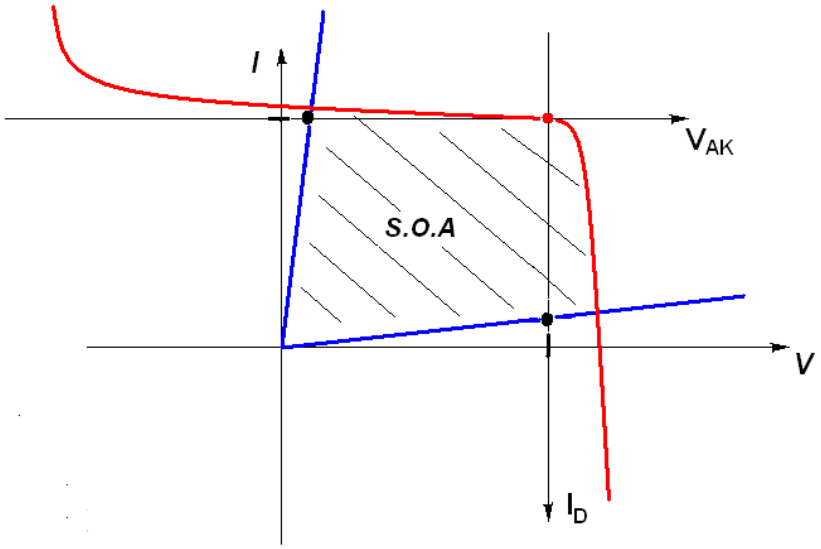


Figure Nº 7: Canonical cell Safe Operating Area.

In order to put both characteristics on same graph the diode characteristic is reversed, seen that works in complement on each commutation, switch state change is done by travelling around the diode characteristic, this commutation is done in a natural way.

Canonical cell defines an operating area practically square; where the switch is able to work without suffer any damage, this area is named SOA and contains the maximum current and voltage values semiconductors can support, those aren't typical commutated current and voltage but over currents and overvoltages should be considered.

As expressed before the analysis done until now is based on an ideal circuit, it means dynamically ideal, actually the commutations occur with a much more complex dynamic caused by all the inductive and capacitive behaviours of components and circuit itself where components are installed.

1.1.2 Reactive Phenomena present on commutations.

1.1.2.1 Dominant Inductive Phenomena:

The reactive phenomena present in commutation circuits are the consequence of the entire connection layout between components forming a commutation loop, those can be represented by a concentrated series inductance to analyze its effects over the components while commutations takes place.

Making a simple analogy, following analysis will be realized with a RL circuit to illustrate effects over the switch caused by the dominance of an inductive characteristic on the circuit.

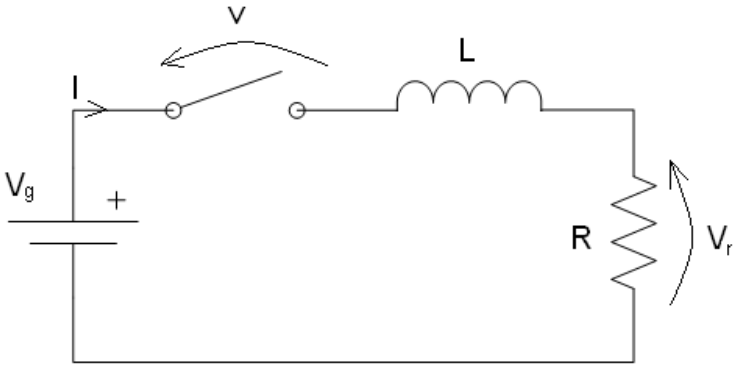


Figure Nº 8: Dominant inductive phenomena circuit.

For the circuits presented in figure 8 is possible to write the following equations:

$$V_g = v + V_L + V_R = v + (\dot{i}) * L + i * R \quad (1)$$

$$v(i) = V_g - (\dot{i}) * L - i * R \quad (2)$$

Where variables of interest are voltage and current on the switch (v, i), state variable is the current (i) considering that circuit is dominated by inductive phenomena.To analyze variables behaviour the SOA waveform is useful because the transition between the switch ON-state to OFF-state and vice versa will be illustrated as a current function.

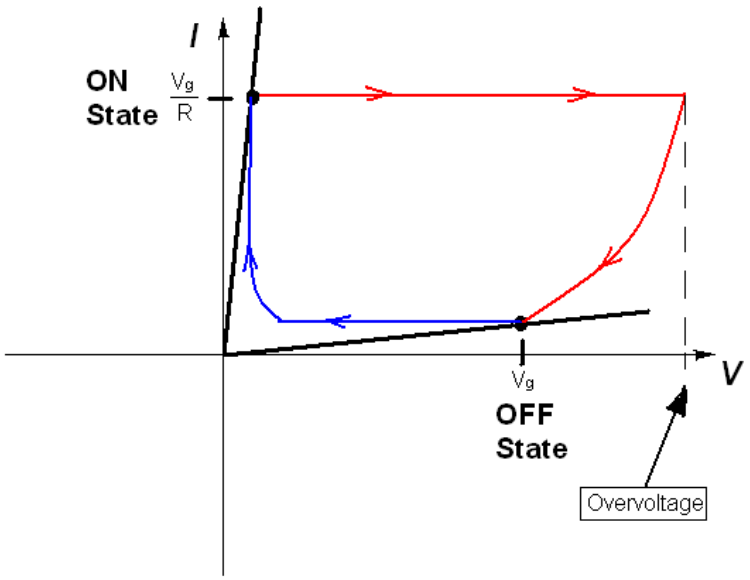


Figure Nº 9: Switch terminals characteristics, dominant inductive phenomena.

With red line switch turn-OFF transition is highlighted, dominated by state variable which is the current.Is possible to see how current remains constant before actually going to OFF-state, this is caused by accumulated energy on the inductance; until the inductance discharge isn't reached switch voltage continues to grow up. This fact not only leads to overvoltage across switch but also to an energetic problem, because while current remains constant the switch terminals voltage is growing so power managed by the switch is greater. This leads to a simple conclusion, if a large inductance is present on circuit the time to discharge it will be also longer so both phenomena impact will increase.

In analogy, with the blue line is highlighted the switch turn-ON transition, being also dominated by the current as state variable in this case the inductive phenomena takes place with a switch lower dissipations and without overcurrent because the turn-ON began with a quasi-zero current value, it remains barely constant while the switch terminals voltage is decreasing.

Obviously is possible to reach the following conclusions, under the dominant inductive phenomena condition:

- The switch Turn-ON commutation is more dissipative than the TURN-OFF one and over voltage on its terminals may occur.
- The switch Turn-OFF commutation is quasi-lossless and overvoltage may not occur.
- The inductance value present in the circuit determinates the commutation switch conditions, the greater the inductance is greater will be the dissipation and the switch terminals overvoltage.

1.1.2.2 Dominant Capacitive Phenomena:

With an analogously simple circuit the effects of the capacitive phenomena will be explained as follows:

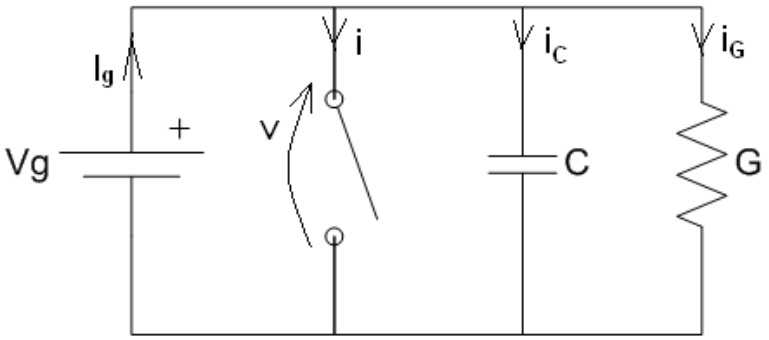


Figure Nº-: Dominant capacitive phenomena circuit.

The next equations are useful to describe the circuit:

$$I_g = i + i_G + i_C = i + v * G + \dot{v} * C \quad (3)$$

$$i(v) = I_g - \dot{v} * C - v * G \quad (4)$$

In this case state variable is the capacitor voltage (v). In every single commutation switch electrical variables are determinate by capacitor state, as shown in figure 10 as follows:

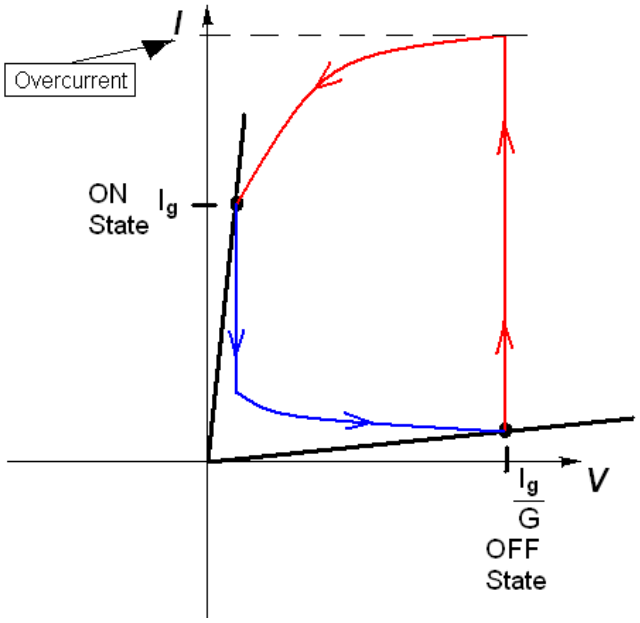


Figure Nº 10: Switch terminals characteristic, dominant capacitive phenomena.

With red line is highlighted switch Turn-ON dominated by state variable, is possible appreciate how voltage across the switch remains barely constant while the current inside the switch is growing up cause by the turning-ON itself and then the voltage goes down to switch conduction threshold, this occurs until the stored energy in capacitor is discharged leading to a possible overcurrent into the switch. Again this phenomenon not only lead to an overcurrent into the switch but also to energetic problems, because the power managed by the switch is greater. Time that capacitor voltage remains constant is proportional to the capacitance present in circuit.

While the blue line highlight switch Turn-OFF, being dominated by the capacitor voltage as state variable, commutation occur with a lower level of dissipation because when switch has to open initial voltage is approximately zero and remains constant motivated by the capacitor, current decrease causing minimum dissipation. Overcurrent may not occur in this commutation.

Obviously is possible reach the following conclusions, under the dominant capacitive phenomena conditions:

- Switch Turn-ON commutation is more dissipative and can lead to overcurrent in the switch.
- Switch Turn-OFF commutation is quasi-lossless and overcurrent may not occur.
- Capacitance present in the circuit determinates the commutation conditions, the greater capacitance is greater will be the dissipation and switch overcurrent.

Analysis done until now is based on a much simpler circuit than real conditions where switches work into canonical cell, but the conclusions are still valid for canonical cells, is important to consider that dominant inductive and capacitive phenomena will not be present simultaneously.

Once these phenomena are clarified may seems logical implement the reactive phenomena in order to reduce switch overcurrent, overvoltage and dissipations;in other words using dominant inductive phenomena in Turn-OFF commutation to eliminate switch overvoltage and reduce dissipation, and using dominant capacitive phenomena for the Turn-ON, reducing switch overcurrent and minimize dissipation. But this is not possible as said previously because dominant phenomena will only be present in one of its forms.

Inductive characteristic in one circuit is caused by connexions between components, represented as a concentrated inductance for academic purposes but actually is a distributed inductance, and can be reduced in design stage looking for layout improvements where canonical cell will be introduced, this implies make components placement in a way that connecting wires are reduced as possible.

In contrast, circuit capacitive characteristic is less manageable because components composition are dominated by this type of phenomena, ON state in power semiconductors is done by holding a minimal voltage between its terminals; when the semiconductor is commanded to make turn-Off, voltage on its terminals increases stimulating field effect which causes a raise into dielectric barrier, this phenomenon produce a growth on the components output capacitance, obviously this behaviour can't be avoided nor the manner of operation.

In conclusion, inductive phenomena can be reduced because they are a layout consequence, making a layout on design stage considering this type of phenomena will lead to a low series inductance on commutation loop avoiding problems related; but capacitive phenomena are inherent to semiconductors nature thru it inner field effect.

1.1.2.3 PWM Ripple Effects

According to modulation canonical cell behaviour is determined; thet next analysis will be done under the PWM (Pulse Width Modulation), typically done with a triangle carrying waveform (tr) and a modulating waveform (M) usually a constant value that can be varied in order to change the canonical cell duty cycle, resulting waveform (r) is the useful command to drive the switch as follows:

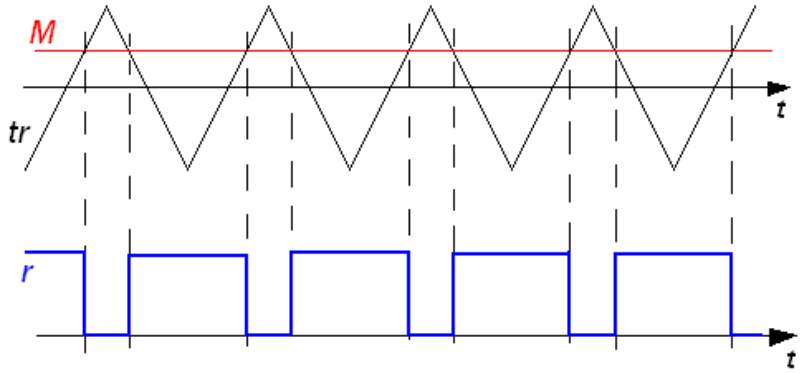


Figure Nº 11:PWM basic waveforms.

For ripple analysis canonical cell will be part of any noted circuit for a DC-DC converter as can be the Buck or Boost configuration or even other possible configuration where the canonical cell is the principal current deviator, to fix the concepts the buck configuration has been taken as example:

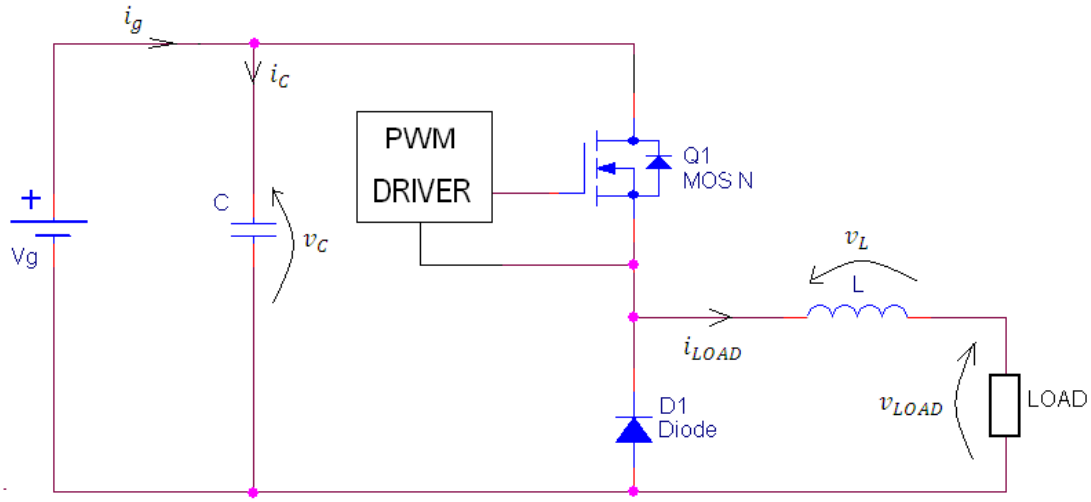


Figure Nº 12: Buck configuration for PWM analysis.

The following equations can be written:

Instantaneous Value Equations:

$$\dot{\varphi} = v_L = r * v_g - v_{LOAD} \quad (5)$$

$$\dot{q} = i_C = i_g - r * i_{LOAD} \quad (6)$$

Average Value Equations:

$$0 = V_L = D * V_g - V_{LOAD} \quad (7)$$

$$0 = I_g - D * I_{LOAD} \quad (8)$$

r is the switch drive variable, while D (Duty Cycle) is it average value.

The average output voltage is represented by: $V_{LOAD} = D * V_g$ (9)

Taking instantaneous value equations is possible to make dynamic analysis of the variables, and highlight the PWM effect over the variables of interest, for every r value [0 or 1] doing equation decomposition is possible to obtain differential equations that governs the system dynamic, some approximation have to be done in order to simplify the analysis; when the r value is 0 the equations became a simply first order but with $r = 1$ they are a second order equations, following graphic summarize ideas, all of them has been simplified to a linear relationship in order to highlight the effects and not their details:

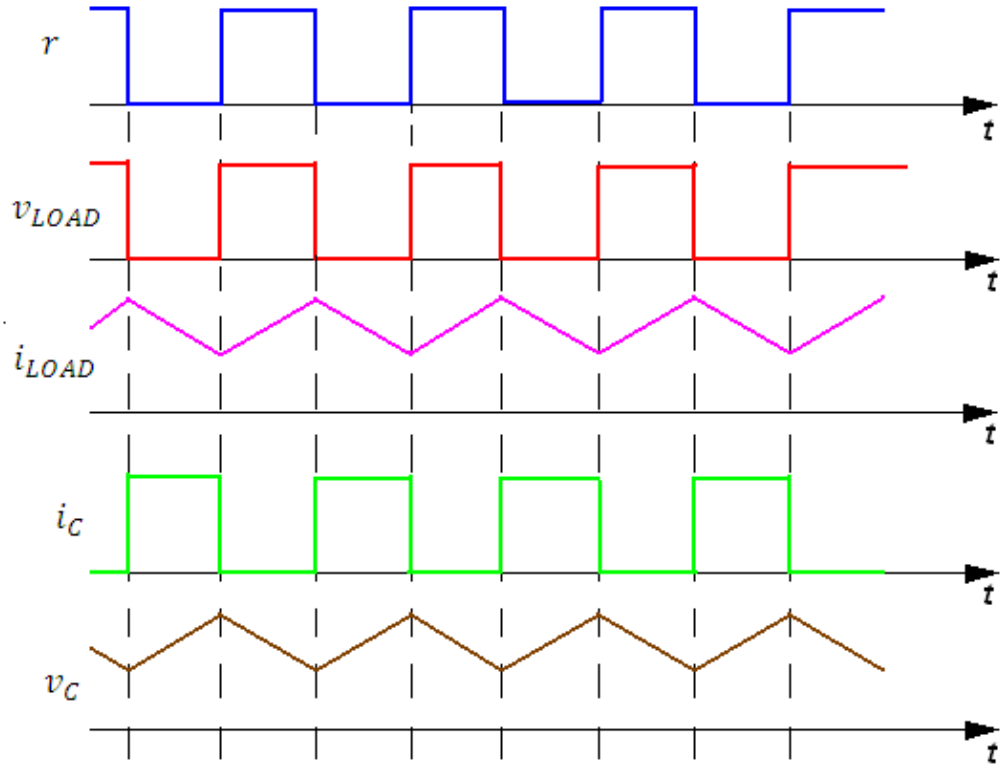


Figure Nº 13: Buck PWM ripple analysis.

When driver variable $r = 0$ the output voltage is approximately equal to the input voltage (assumed constant in first approximation) while load current has a positive slope dominated by the output inductance response to output voltage, on the other hand we have positive capacitor current discharging it, decreasing voltage with a negative slope delivering it energy to the load.

For the second semi period, when $r = 1$ output voltage is minimal because freewheeling diode is active, and load current decrease from the maximum current to a minimum value; on the input side while the switch is open

current generator flows directly into the capacitor charging it until it maximum level.

An approximation was done, figure 13 shows a constant output voltage when switch is ON, is possible to see the input voltage decrease caused by the discharge of capacitor then output voltage will have the same waveform than input voltage when $r = 1$, this approximation was done to have a starting point for the analysis.

Obviously, as shown the PWM creates a ripple over input voltage and output current as illustrated before, this fact motivates a different treatment of the SOA because the switched voltage and current will be higher. Then switched voltage ($(V_C)_{MAX}$) should consider not only input average value (V_C) but also ripple magnitude, just same reasoning is valid for switched current ($(I_L)_{MAX}$), SOA will be modified as follows considering the "u" and "a" parameters to quantify the voltage and current ripple respectively named ripple factors.

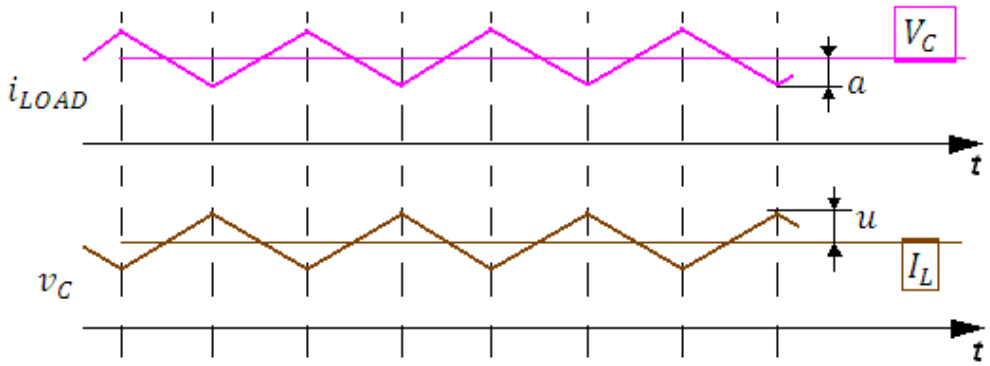


Figure Nº 14: Input voltage and output current ripple

$$(V_C)_{MAX} = V_C(1 + u) \qquad (10)$$

$$(I_L)_{MAX} = I_L(1 + a) \qquad (11)$$

The resulting SOA shown in figure 15 considering the ripple will be wider, so components used should manage higher power respect not having the PWM ripple effects, as said before the SOA is determined by switched current and voltage but in this case those values are higher than average value.

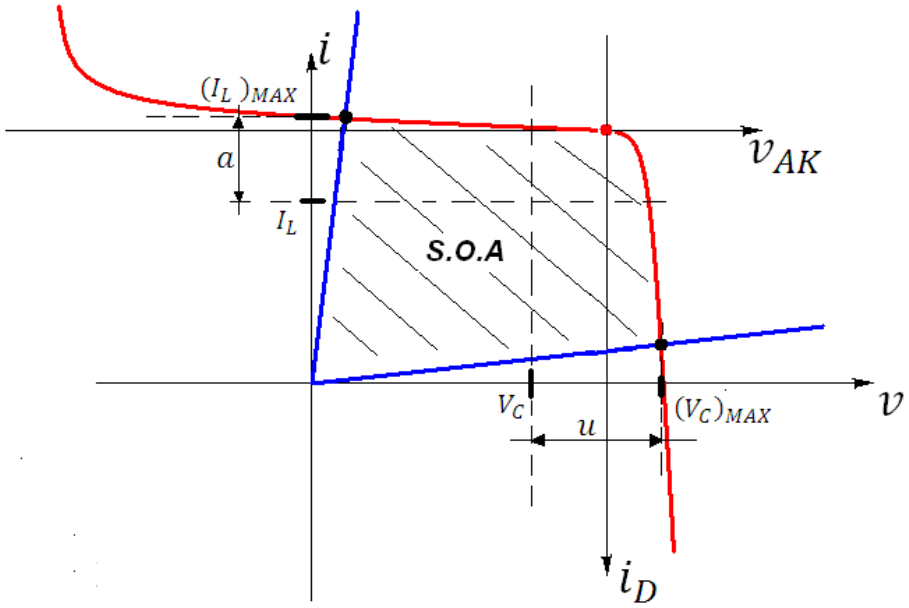


Figure Nº 15: SOA considering ripple effects.

Ripple factors will be determined in design phase according to an analysis linked to converter application, and will be decisive for components selection; higher are ripple factors, higher will be power dissipation on components just as current and voltage capability, clearly explained in figure 15.

1.1.3 Mosfet and Diode technologies actually used

In the present market many technological methods for power components construction exists, on the next study state of the art is presented and analyzing general behaviour of canonical cell under real conditions.

1.1.3.1 Diodes:

Is necessary to know typical characteristics of diodes just as:

- Continuous Forward Current (I_F)
- Forward Voltage (V_F)
- Reverse Current (I_R)
- Reverse Voltage (V_R)

On power electronics also is necessary to know the dynamic characteristics as the Reverse Recovery Charge (Q_{RR}), Reverse Recovery Time (t_{RR}), and the Output Capacitance Variation. These concepts will be treated immediately.

1.1.3.1.1 Reverse Recovery Charge (Q_{RR}), Current (I_{RR}) and Time (t_{RR}), and Softness Factor:

When a power rectifier is quickly reverse biased while is conducting a high forward current (hard switching), a finite amount of time is required to clear it of charge carriers so that it can block the reverse voltage. The amount of time it takes a hard-switched rectifier to recover (t_{RR}) has been the typical performance metric used to evaluate rectifier reverse recovery. However, the amplitude of the reverse current that flows through the rectifier during the recovery time (I_{RR}) is a better measure of the performance in a power conversion circuit than (t_{RR}) alone.

A rectifier's reverse recovery characteristics are quantified by three parameters: the reverse recovery time (t_{RR}) the reverse recovery current (I_{RR}), and the reverse recovery charge (Q_{RR}), Q_{RR} , t_{RR} and I_{RR} are the three main parameters that are used to characterize the rectifier's reverse recovery behaviour, and are typically specified on the datasheet. Another parameter that is not always specified on the datasheet is the softness of the rectifier's I_{RR} waveform. Those four parameters are determined by the manufacturing processes used to produce a particular device family.

The Q_{RR} (the integral of the recovery current over the recovery time) of a power rectifier is a direct measure of its stored charge, which must be removed so that the depletion region can become big enough to block the reverse voltage. Semiconductor design engineers can use various techniques to control the duration or the lifetime of minority carriers.

Softness is the ratio of the two parts of the reverse recovery current: stored charge removal (called Storage) and the return to zero current (called Transition). Softness is calculated by dividing the time required to remove the stored charge carriers from the diode (t_a) into the time it takes for the resultant reverse current to fall from its peak negative value (I_{RR_PEAK}) back to zero (t_b).

Softness = t_b/t_a, and the parts of the waveform are shown in figure 16. The softness of a device's I_{RR} will depend on the lifetime control technique used to reduce Q_{RR}. The softness factor can easily be calculated for rectifiers that do not have this parameter specified in their data sheets.

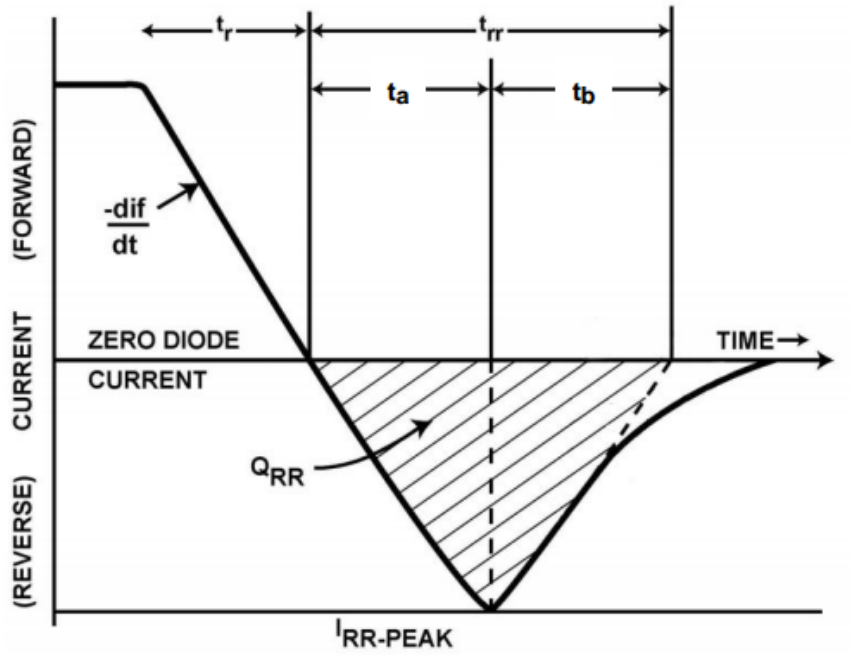


Figure Nº 16: An I_{RR} waveform showing the storage and transition that make up the softness ratio.

Is important to say that abrupt recovery also produces excessive EMI (Electromagnetic Interference) and voltage stress across the rectifier, which requires snubber circuitry or larger EMI filter components. Soft recovery reduces voltage stress and EMI, without the use of snubbers.

1.1.3.1.2 Non linear Output Capacitance

Reverse recovery phenomenon together with field effect inside semiconductor produce a capacitance dynamic while voltage increase, in first place charge that has to be deliver to block the voltage initially depends on the reverse recovery effects, and then when component is already open the junction remains producing a quasi-constant output capacitance, these phenomena are not always the same and they will vary according to the used construction technology or diode nominal parameter, as shown in figure 18 and 19 token directly from the IDH16S60C16A-600V Schottky Diode Datasheet made by Infineon, and FFPF30UA60S 30A-600V Silicon Diode Datasheet made by FairChild Semiconductors respectively.

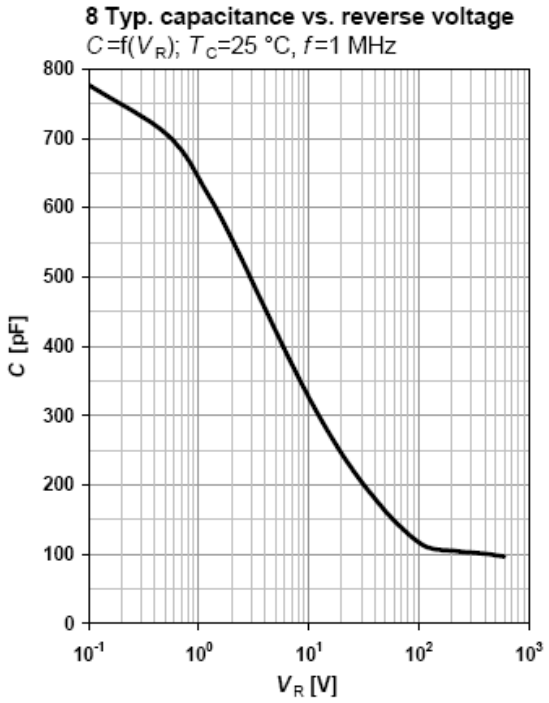


Figure Nº 17:IDH16S60C 16A-600V Schottky Diode junction capacitance.

Figure 3.Typical Junction Capacitance

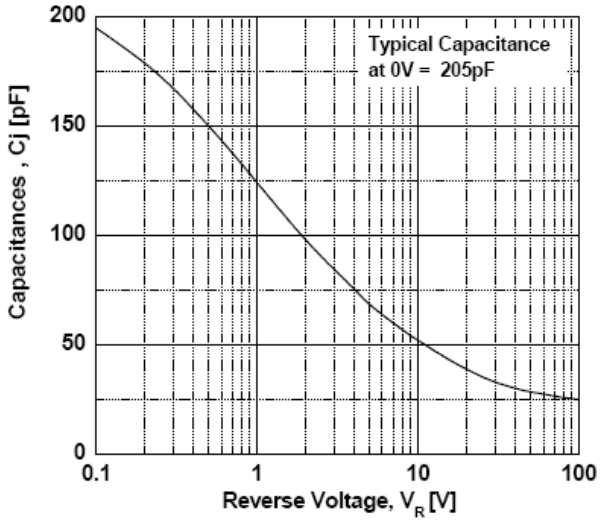


Figure Nº 18:FFPF30UA60S 30A-600V Silicon Diode junction capacitance.

From both figures is important to see variation of capacitance as function of reverse voltage applied, Schottky diode presents a capacitance variation from approx. 800pF at 0,1V to approx. 100pF at 100V and Silicon diode which capacitance goes from quasi 200pF to 20pF with same reverse voltage applied, and then both capacitance remains quasi constant from 100V onwards.

1.1.3.1.3 Constructive Diode Technologies:

Silicon Diodes: also known as p–n junction diode, is made of a crystal of semiconductor. Impurities are added to it to create a region on one side that contains negative charge carriers (electrons), called n-type semiconductor, and a region on the other side that contains positive charge carriers (holes), called p-type semiconductor. When two materials n-type and p-type are attached together, a momentary flow of electrons occur from n to p side resulting in a third region where no charge carriers are present. It is called Depletion region due to the absence of charger carrier (electrons and holes in this case). The diode's terminals are attached to each of these regions. The boundary between these two regions, called a p–n junction, is where the action of the diode takes place. The crystal allows electrons to flow from the N-type side (called the cathode) to the P-type side (called the anode), but not in the opposite direction.

Is the basic technology used to manufacture diode, some improvements has been done on time, improving their principal parameters as forward voltage, forward current, reverse voltage, reverse current, reverse recovery charge, time and current according to the applications.

Schottky diodes: are made with ametal–semiconductor junction formed between a metal and a semiconductor, creating a Schottky barrier (instead of a semiconductor–semiconductor junctionas in conventional diodes). Typical metals used are molybdenum, platinum, chromium or tungsten; and the semiconductor would typically be N-type silicon. The metal side acts as the anode and N-type semiconductor acts as the cathode of the diode. This Schottky barrier results in very fast switching and low forward voltage drop. A normal silicon diode has a voltage drop between 0.6–1.7 volts, while a Schottky diode voltage drop is between approximately 0.15–0.45 volts. This lower voltage drop can provide higher switching speed and better system efficiency. Not always Schottky diode has lower voltage drop than Silicon diodes.

The most important difference between the p-nand Schottky diode is reverse recovery time, where in a p-n diode the reverse recovery time can be in the order of hundreds of nanoseconds and less than 100 ns for fast diodes, Schottky diodes do not have a recovery time, as there is nothing to recover from (i.e. no charge carrier depletion region at the junction). With p-n junction switching, there is also a reverse recovery current, which in high-power semiconductors brings increased EMI noise and increase power dissipation. With Schottky diodes switching essentially instantly with only slight capacitive loading, this is much less of a concern.

SiC Schottky diodes: constructed fromsilicon carbidehave a much lower reverse leakage current thansiliconSchottky diodes, and higher reverse voltage, within a decrease of the reverse recovery parameters.

1.1.3.2 MOSFETS:

Just as with diodes there are different Mosfet constructive technologies, differentiated by used materials or constructive techniques, they are:

- Si Mosfet Conventional planar technology: Typically have a high R_{DS} per unit area, and thus require large die sizes to achieve a low $R_{DS_{(on)}}$. However, a larger die size has lower current density, and better heat sinking capabilities.
- SiC MosfetConventional planar technology: Manufactured with Silicon Carbide presents a lower $R_{DS_{(on)}}$ than Silicon Mosfet having the same die size, also the body diode performance is improved reducing the Reverse Recovery parameters.
- TrenchGate Mos or Trench Mos: This type of mosfet uses a new structure to provide a more direct and hence more efficient path for the current flow within the semiconductor device. The low resistance of the TrenchMOS FETs means that heat sinks are not required in many instances, enabling these devices to be made in smaller packages.

The previous comparison was made is base of their constructive and$R_{DS_{(on)}}$differences, but there are many other characteristic that defines the Mosfet uses, as the output capacitance which determinates its dynamical behaviour during commutations.

Non linear capacitance are present in both Mosfet and Diodes, as seen before diodes initially have a large output capacitance until certain reverse voltage where the capacitance became smaller, because the field effect is the same in semiconductor the only substantial difference is the magnitude of the output capacitance, for Mosfet this phenomena isgreater than diodes. This fact is shown in figure 19 with the output capacitance (C_{OSS}) present in the 500V-60A-0,045mΩ ST Silicon Mosfet STY60NM50, where the initial value is approx. 2nF and the final value with a 50V reverse voltage is quasi zero capacitance, the variations are more abrupt than diode characteristic.

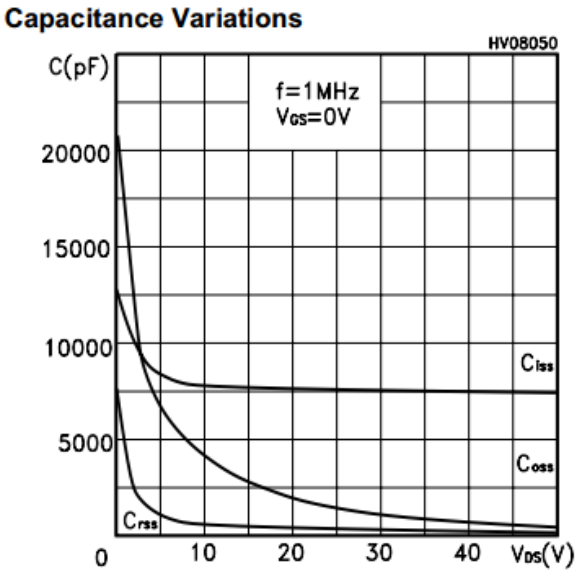


Figure Nº 19:STY60NM50 60A-500V Silicon Mosfet capacitance variations.

1.1.4 Commutation General Behaviour (Turn-ON & Turn-OFF)

Taking into account the dynamic problems the commutation transitions are affected, the analysis will be done immediately to illustrate the general behaviour of the canonical cell commutations.

1.1.4.1 Turn-ON analysis

In the first place the Turn-On commutation will be considered, when the freewheeling diode conduces the load current and the switch is turn-on commanded. Initially theV_{DS}(Drain-Source voltage) is maximal, it's equal to the generator voltage, then the V_{GS}(Gate-Source voltage) is increased in order to close the switch, this process is illustrated in figure 20 as follows:

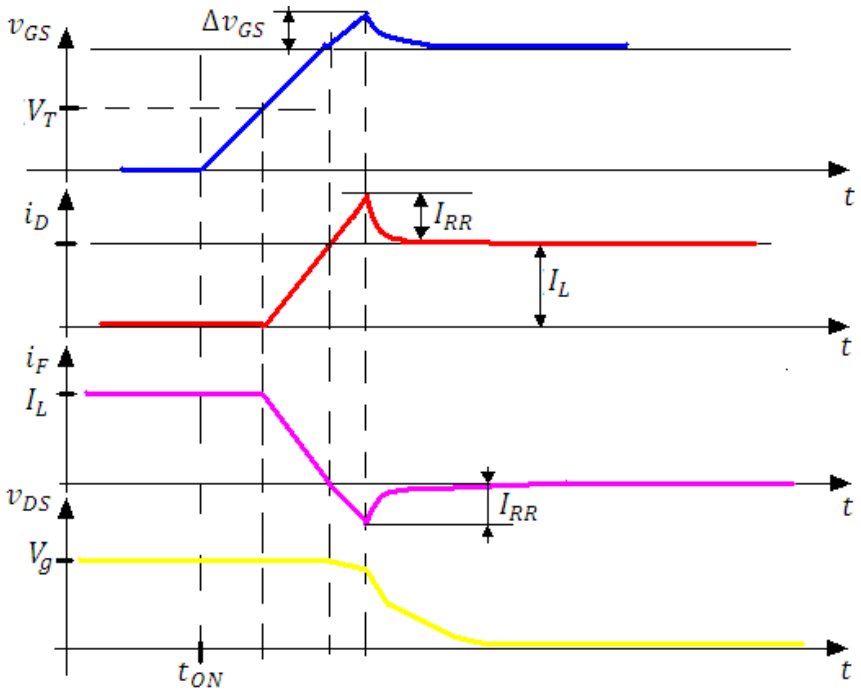


Figure Nº 20: General turn-ON canonical cell behavior.

When the v_{GS} start to increase (t_{ON}) will not have effect into the drain current conduction until it reach the threshold voltage (V_T), once v_{GS} is greater than the threshold the drain current (i_D) will start to increase approximately with a constant slope; arriving to the load current value (I_L) the diode is passing from it conduction state to it interdiction state ($i_F = 0$) then the reverse recovery phenomenon has place, the diode is passing through zero currentbut still must conduce the reverse recovery current (I_{RR})necessary for the storage. The switch must conduct the diode reverse recovery current until is open; this phenomenon leads to an overcurrent into the Mosfet that should be also considered in the sizing of the SOA. Once the current is completed the v_{DS} starts to decrease with to different slopes, the first part is due to the linear capacitance of the canonical cell ($\dot{v_{DS}} = \frac{I_{R\square}}{C_{Linear}}$) in part dominated by the diode reverse recovery, then when the recovery is finished the second part of the voltage transition will be done with both constant capacitance (Mosfet and diode).

The increase seen in the gate-source voltage final part is caused by the gate-drain transconductance which increases the gate voltage even when the command variable is constant v_{GS}.

Then a simple conclusions will be reached, the diode reverse recovery leads to and Mosfet overcurrent and also increase the power dissipation into the Mosfet because a higher current is been conducted with the nominal voltage over the switch.

1.1.4.2 Turn-OFF analysis

Now the turn-OFF commutation will be analyzed, under the same principles, the command variable is given to the gate and then a series of event takes place, these can be seen in figure 21:

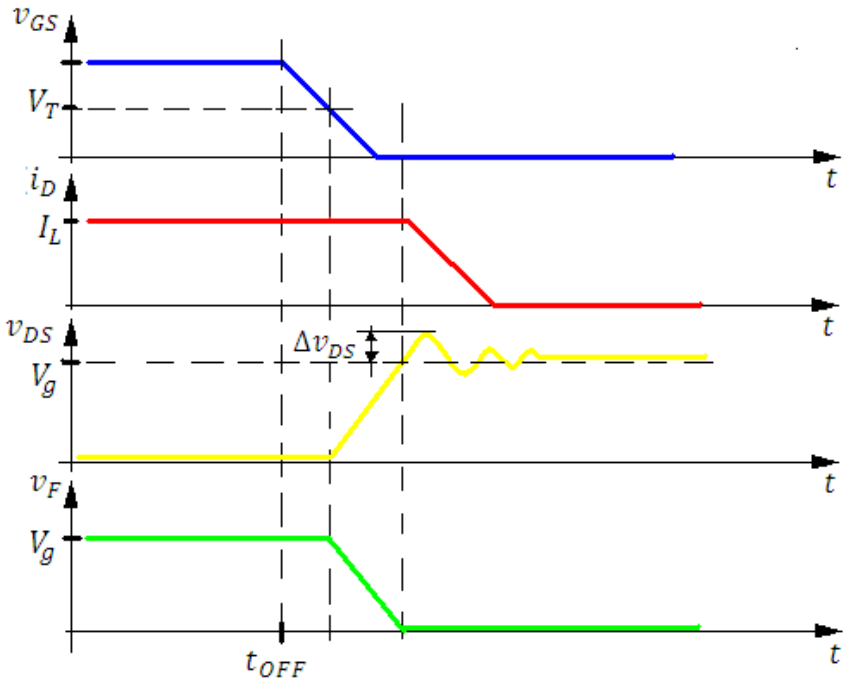


Figure Nº 21: General turn-OFF canonical cell behavior.

The gate-source voltage (v_{GS}) should be lower than the threshold voltage (V_T) to start the switch turn-OFF, then voltage transition will start increasing the v_{DS} caused by the drain-source releasing, across the diode the voltage will decrease (v_F) in a complementary way respect the drain-source voltage. Once the voltage transition is completed the current transition will start with a current reduction on the Mosfet (i_D) and an analogously current increase inside the diode (i_F). Is important to note the Mosfet output voltage (v_{DS}) will increase above the generator voltage (V_g) caused by the resonance between the output capacitance and the series inductance present into the commutation loop, this phenomenon will lead to an overvoltage across the Mosfet (Δv_{DS}) and not only, also increase the Mosfet power dissipation.

1.1.4.3 SOA Modification

In both cases SOA will be affected, in the first one caused by the reverse recovery which forces an overcurrent into the Mosfet, and the second one is

disturbed by the possible overvoltage across the Mosfet, these modifications are illustrated bellow:

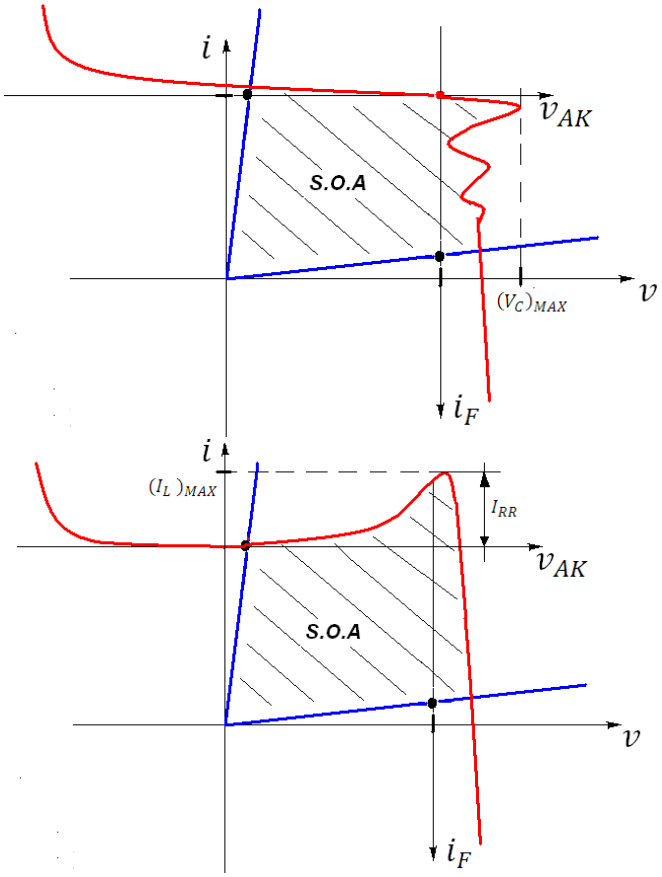


Figure Nº 22:SOA individually modified by real behavior of components.

Reverse recovery effect should be avoided, otherwise the switch commutated current will be greater, causing an over sizing of the Mosfet in this case and more power dissipation. The inductive effects can be avoided as said before making a correct layout design.

1.1.5 Trench Mosfet used in Switched Mode Power Supply (SMPS)

For very low voltage application (<100V) and Discontinuous Conduction Mode (DCM: Pulsed Current) the canonical cell used is not formed by a mosfet and diode, but with two mosfets (figure 23), this choice leads to a different form of operation. The turn-On and Turn-Off will be explained immediately:

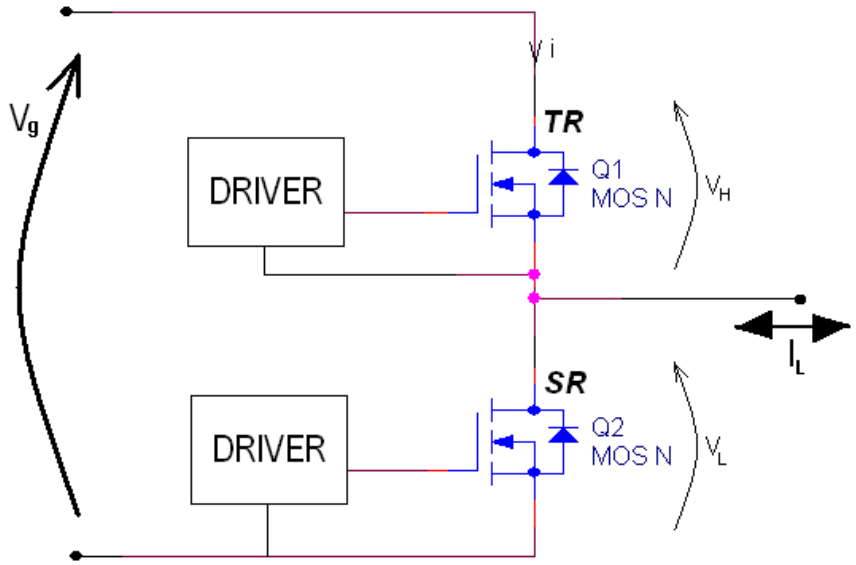


Figure Nº 23: Canonical cell used for DMC SMPS.

Both Mosfet will not been called equally, because their operation manner is different, the superior one will be named as TR (transistor) and the inferior one SR (Synchronous rectifier), the Turn-ON and Turn-OFF commutation will be referred to the TR.

Output Current characteristic in DCM is illustrated bellow:

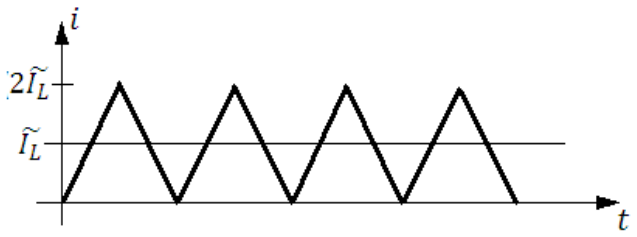


Figure Nº 24:DCM current waveform.

Initially is important to introduce the synchronism problem with both switch commutation to reach the perfect current deviation objective of the canonical cell, when the Turn-OFF is done, the current should flow inside the SR, and for the Turn-ON the current should move from the SR to the TR.

The turn-OFF commutation will be made at the maximum current ($i = 2\tilde{I}_L$) and then TR is commanded to its OFF state, the voltage across the TR (v_H) starts to increase loosely with constant slope while the voltage across the SR decrease dominated by the body diode, once the voltage transition is finished the load current (i_L) start to flows inside the SR Body Diode (used specially motivated by its electrical characteristics, being a TrenchMos, as can be low conduction drop) and once the current transition into the TR is done the SR is

commanded to its ON state, this transition became naturally just as in the state of the art canonical cell (Mosfet-Diode) because of the presence of the body diode, otherwise the synchronism is required (Figure 25).

The turn-ON commutation is a little bit difficult respect to the other one, motivated by the non linear output capacitance of the SR, if the system operation wasn't DCM the TR should deliver together with the load current all the charge necessary for the reverse recovery and the linear capacitance, but working in DCM the Turn-ON commutation is done when the output current is null (consequently the SR current (i_{SR}) and TR (i) are null), then the load is the responsible for delivering the storage charge (Figure 25).

This fact starts a resonance which increase the voltage across the SR (v_L) (resonance between the output inductance and the SR linear capacitance), while this happens the voltage across the TR (v_H) is decreasing, the TR driver has to be smart enough to identify the maximum voltage and command the Turn-On which will be realized with minimum commutated voltage across the TR without any current inside itself, minimizing the losses.

In the successive semi-period the TR must conduct greater current than ($2\widetilde{I_L}$) in order to deliver not only the load current but the charge lost by the load during the diode storage.

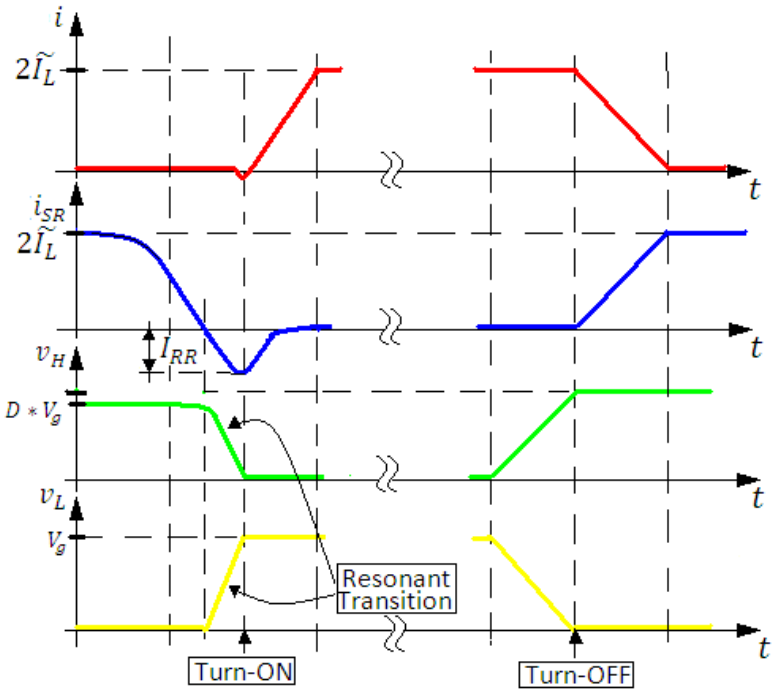


Figure Nº 25: Turn-On/Off current and voltage transitions.

To make even clearer the turn-ON losses reduction, figure 26 illustrates the SOA resulting of the SMPS working in DCM, the OFF transition is done along the SOA because the commutation is made naturally using the SR body diode, while the Turn-ON transition is made almost travelling the axis with quasi-zero voltage and quasi-zero current, this commutation is called lossless and is specially used for energy saving or green technologies.

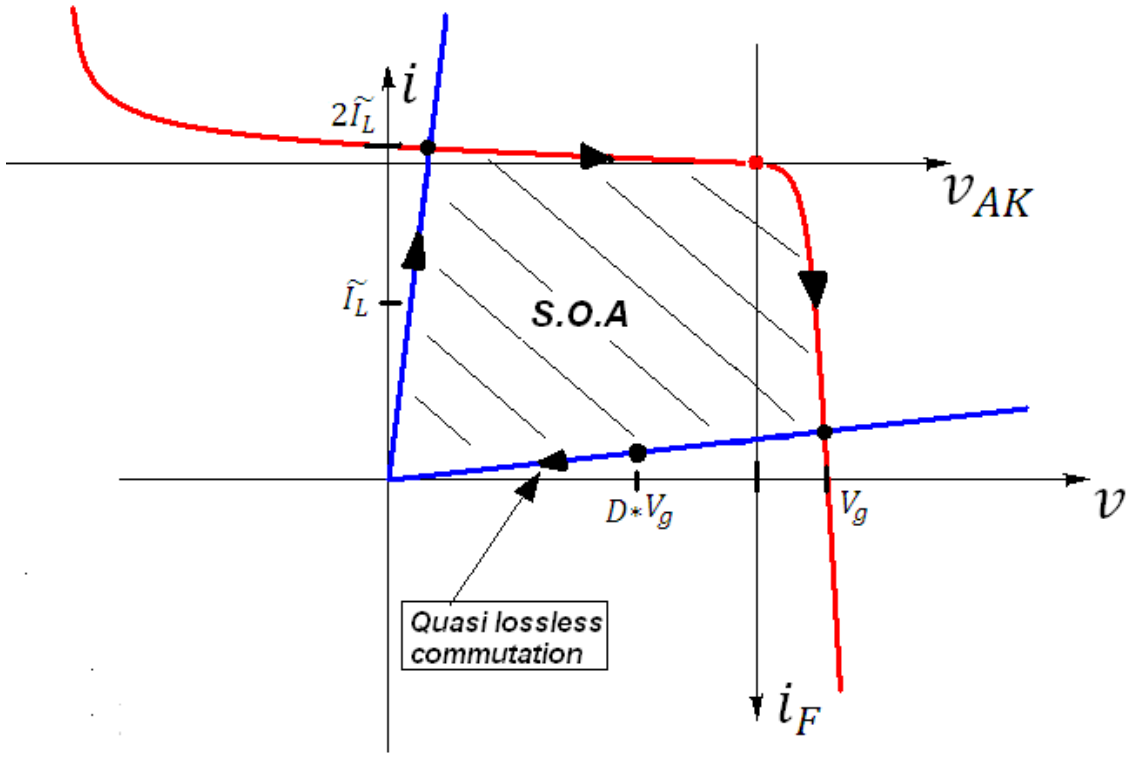


Figure Nº 26: SOA under DCM for SMPS.

1.2 INVERTER LEG STATE OF THE ART

For low voltage application (>100V, <1000V) the inverter leg state of the art is constructed with two unidirectional canonical cells with opposite currents, in this way the resulting leg is current bidirectional and unipolar, the switching components used are IGBT's with Schottky Diodes.

The IGBT for low voltage are more controllable than low voltage Mosfet (extremely non linear output voltage variations), this is the principal reasons for which this switches are chosen, but typically present a higher conduction voltage drop respect power Mosfets (around 1,5V and 2V). Schottky diodes are the chosen complementary semiconductor due to its dynamic and static characteristics; they present a low voltage drop (around 1,5V) and a negligible

reverse recovery. With these components the state of the art inverter leg (shown in figure 27) is used for AC conversion.

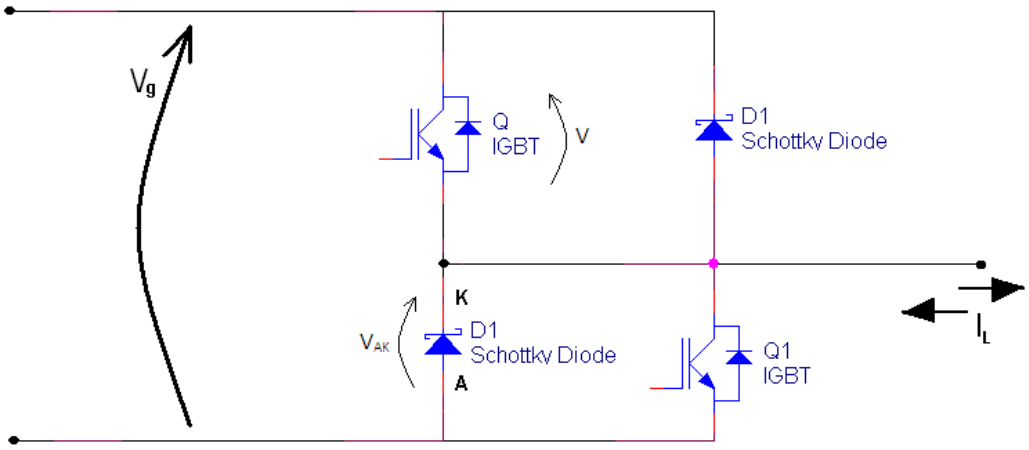


Figure Nº 27: Inverter leg state of the art.

As example one IGBT has been chosen (IR IGBT 600V 34A AUIRG4BC30S-S) to show the $(v_{CE})_{SAT}$, which determinates the conduction losses, and the output capacitance in order to compares it with the Mosfet non linear output shown previously.

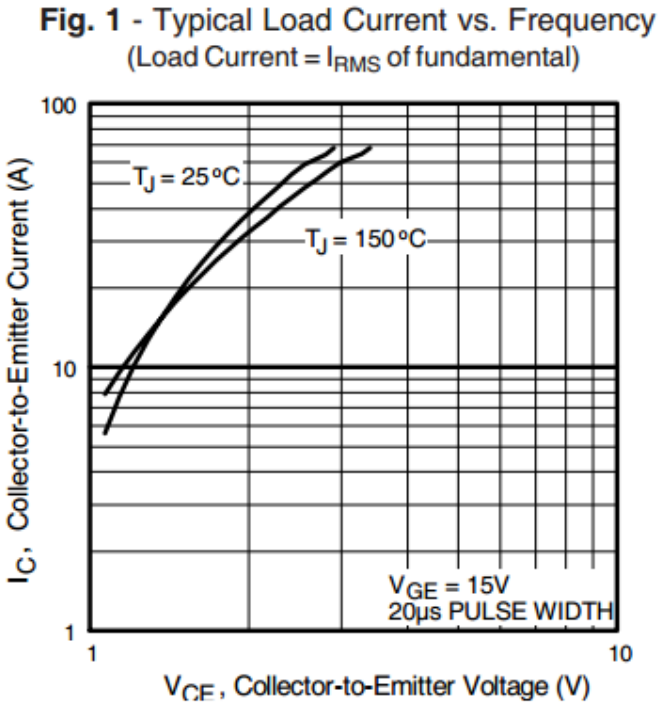


Figure Nº 28: IGBT Collector-Emitter Voltage drop vs. Collector Current (AUIRG4BC30S-S).

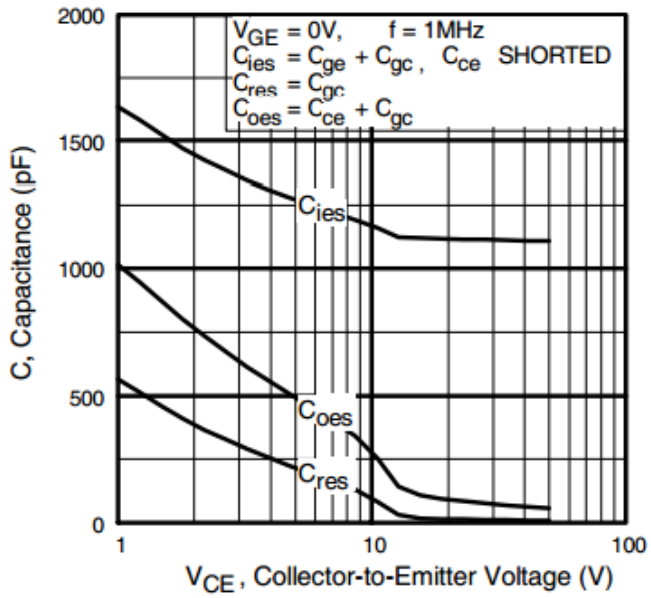


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

Figure Nº 29: IGBT output capacitance (AUIRG4BC30S-S).

Is possible support with the two figures below the $(v_{CE})_{SAT}$ and the output capacitance characteristics, $(v_{CE})_{SAT}$ conducing 10A is over the 1,2V, and the output capacitance is less abrupt in its variations.

To confirm the difference between IGBT and mosfet, one Mosfet datasheets is consulted (ST Mosfet 600V 33ASTP42N65M5), with figures 30 and 31 are reported the $(R_{DS})_{ON}$ and the output capacitance characteristic respectively. The $(R_{DS})_{ON}$ in the Mosfet conducing 10A is approximately 0,068Ω giving as consequence a 0,68V drop. The output capacitance varies two magnitude orders in less than 20V while the IGBT does it in around 50V with a much softer slope.

Figure 11. Static drain-source on resistance

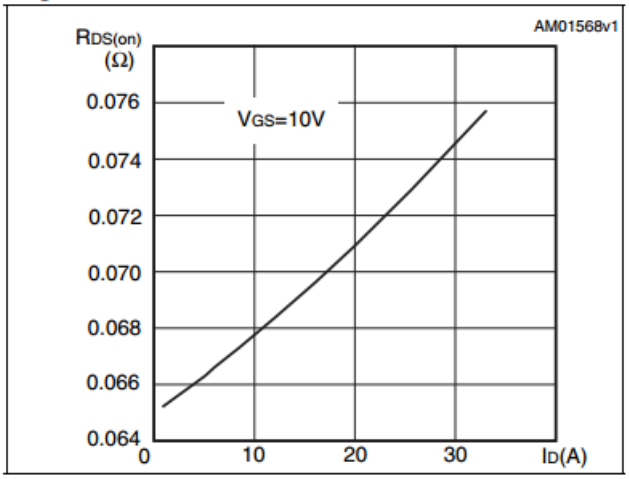


Figure Nº 30: Mosfet $(R_{DS})_{ON}$characteristic (STP42N65M5).

Figure 12. Capacitance variations

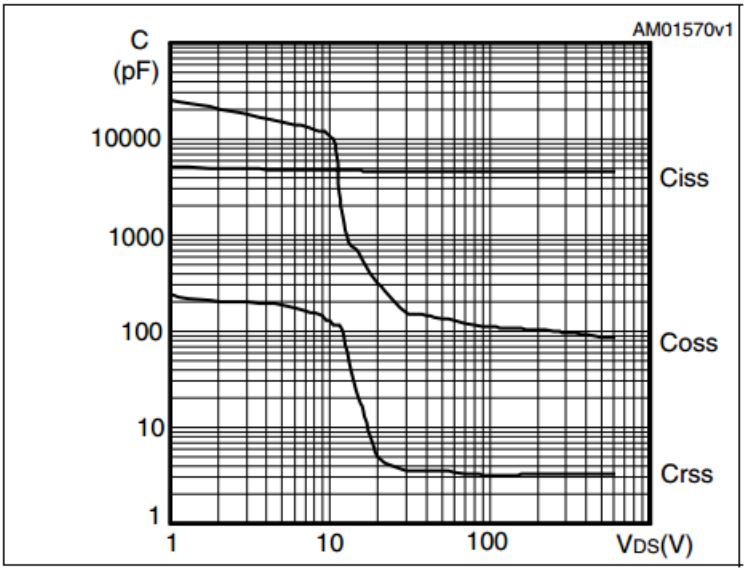


Figure Nº 31: Mosfet output capacitance (C_{OSS}) (STP42N65M5).

1.3 THE SIMPLEST VOLTAGE SUPPLIED INVERTER LEG

To reach current bidirectionality the inverter leg state of the art uses 4 component, with specialized functions, the next proposal minimize the number of useful components from 4 to 2, maintaining all the functions of an inverter leg. Constructing the inverter leg with 2 Mosfets is the simplest way to achieve the new state of the art inverter leg as follows:

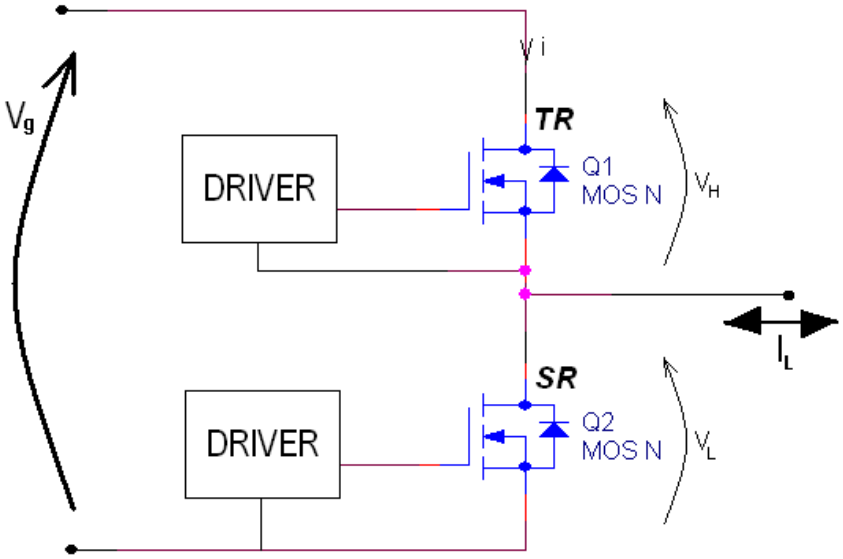


Figure Nº 32: The simplest V.S inverter leg.

1.3.1 Duality with the First Successful Commutation Structure

Over the years, power static conversion has been done with a canonical cell formed by two identical components which allows electrical engineers to solve any conversion problem, passing for AC-AC conversion including rectifiers (AC-DC) and inverters (DC-AC). The canonical cell used is based on two Thyristor or SCR (Silicon-controlled rectifier) having the characteristic of being voltage bipolar and current unidirectional. Where each component has a 1st and 3rd quadrant useful characteristic, this canonical cell is shown in figure 33.

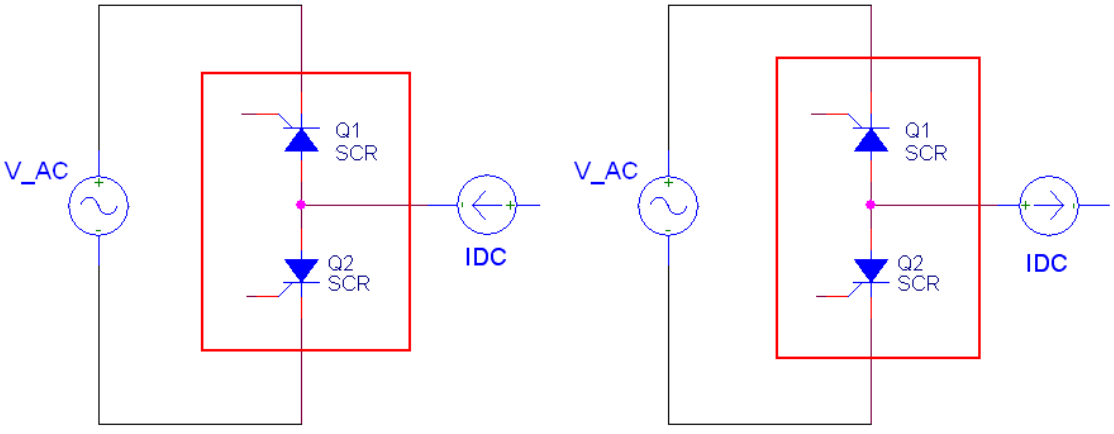


Figure Nº 33: Thyristors based canonical cell for DC-AC and AC-DC conversion

The principal idea which supports he analogy of the 2-Mosfet inverter leg with the 2-thyristors canonical cell is functional duality, both fundamental components has a 1st and 3rd quadrant useful characteristic but in dual variables, as current and voltage; this fact allows the passage from Current Supplied to Voltage supplied functionality.

1.3.2 The reason why 2-mosfet inverter leg has not being used so far

Non linear output capacitance has a very important role when dynamic is necessary, this phenomenon has been treated previously in the present study with the DCM for very low voltage DC-DC conversion applications (chapter 1, Section 1.1.5).

Low voltage applications with a medium to large power conversion doesn't work in DCM but in CCM (Continuous Conduction Mode), in other word when switches are turn-ON commanded they must not only handle the load current but also the reverse recovery current and the linear initial charge necessary to open the complementary switch which works as synchronous rectifier.

Based on the proposed inverter leg (figure 32) analysis will be done for each commutation (Turn-ON and Turn-OFF), where both Mosfet will not be called equally, the superior one will be named as TR (transistor) and the inferior one as SR (Synchronous Rectifier) motivated by the role that each one plays. Turn-ON and Turn-Off will be only referred to the TR.

Turn-OFF analysis: this particular commutation analysis will be performed similarly to the DCM of a SMPS done before, when the TR is commanded to OFF the voltage transition will starts motivated by the drain-source release, once this transition is finished the current transition has place forcing the SR body diode to conduct the load current, which will respond naturally to the stimulus. After the current transition is done the SR will be commanded to its ON state. Synchronism between the TR and SR command isn't required. Only when large current must be interrupted problems will appear because the commutation will cause larger $^{dv}/_{dt}$, leading to EMI problems.

Turn-ON analysis: keeping the freewheeling transistor ON the turn-ON command arrives to the TR, the reverse recovery into the SR shall be completed simultaneously to the linear capacitance transition requiring a charge not negligible but appreciable, this charge must be delivered by the generator and not by the load (as the DCM case) so the TR in the first stage of it current transition must conduct the load current (I_L) plus the reverse recovery current (I_{RR}), this stage is done with a modest $\frac{dV}{dt}$ because of the large leg capacitance, then the leg

capacitance became smaller suddenly and the $\frac{dV}{dt}$ will became extremely steep leading to EMI. Figure 34 illustrates the turn-on dynamic which is pretty similar to the turn-on commutation explained in Chapter1-XXX for the Canonical cell general behaviour, with a major difference, non linear output capacitance phenomenon are greater, that's why the EMI will be a problem.

In order to decrease the possible EMI derived by hard-switching, drivers must command a soft turn-ON with dominated transitions leading to major power dissipation, so if hard-switching is adopted for the simplest inverter leg EMI can arises, the solution is to slow down the driving, accepting a power dissipation increase. **This leads to a paradox, faster components as the actual Mosfet must be driven slower**.

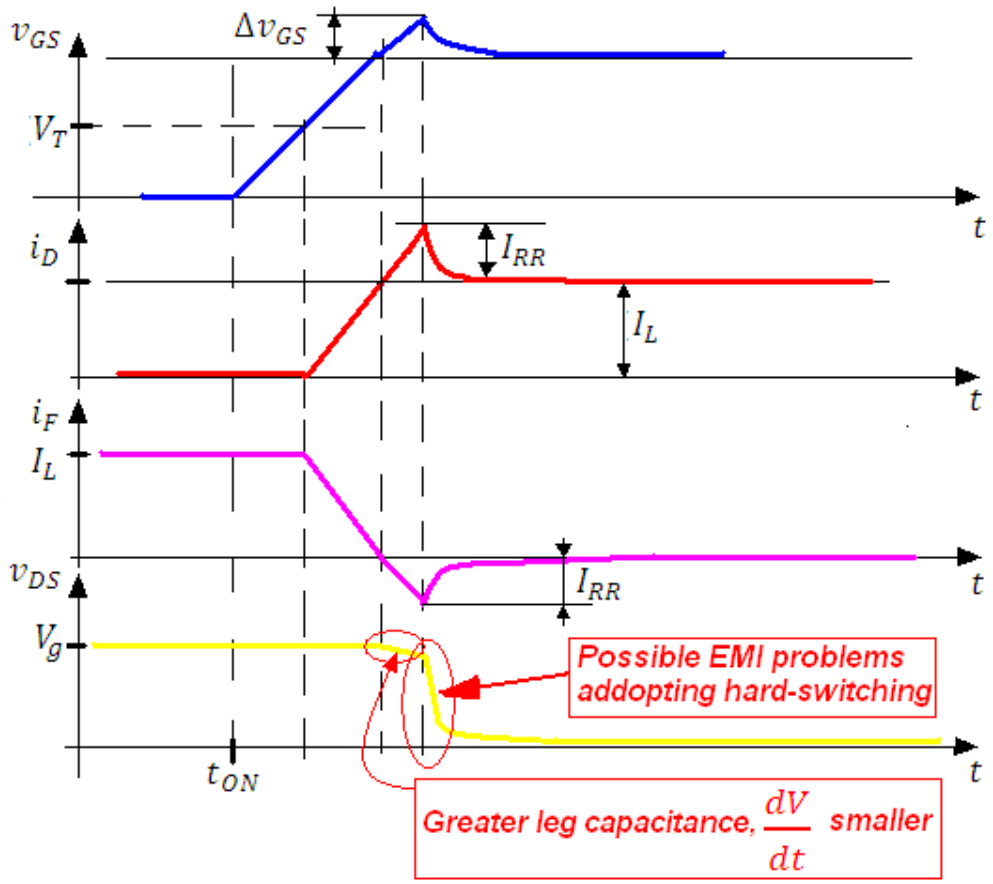


Figure Nº 34: General behaviour adopting hard-switching with the 2-mosfet inverter leg

CHAPTER II

THE 2-MOSFET VOLTAGE SUPPLIED (V.S) INVERTER LEG (I.L)

2.1 Conduction Advantages

State of the art Inverter Leg (S.A.I.L) vs. 2-Mosfet I.L

Before further progress in important to highlight the conduction characteristics are presented by the 2-mosfets I.L with respect to the State of the Art I.L (SAIL), as seen before the SAIL is constructed using two IGBTs and two Schottky Diodes these components presents a well defined conduction voltage drop which contrasted with the Mosfet conduction characteristic aren't very different.

For the 2-mosfet I.L each single components substitute the IGBT or the Schottky diode according to the leg working conditions, by this reason a comparison will be done in terms of conduction voltage drop between one specific chosen Mosfet and one IGBT, and then also compares the Mosfet with Schottky diode in order to verify the conduction losses differences between the two different legs.

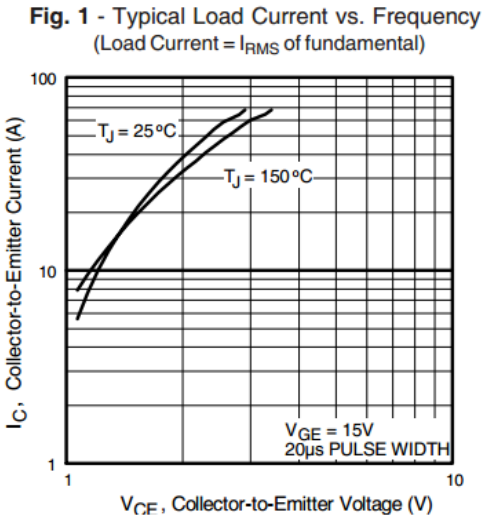
In Chapter I a contrast was done between IGBT and MOSFET in term of conduction voltage drop and output capacitance as an introductive analysis to chose MOSFET instead IGBT into the Simplest Inverter Leg, in the next paragraph same transistors will be compared to estimate the conduction losses, and also the Infineon 600V 16A IDH16S60C Schottky Diode has been chosen to complete the SAIL (IBGT-Schottky), at less two diodes must be used in parallel to reach the IGBT's current capability (34A).

Conduction voltage drops are shown below taken from each datasheet available on internet; IGBT $(V_{CE})_{SAT}$and MOSFET $(R_{DS})_{ON}$ are reported again in figure 35 and 36 respectively, and finally Schottky diode forward voltage is shown in figure 37 as follows:

IGBT: IR 600V 34A AUIRG4BC30S-S.

MOSFET: ST 600V 33A STP42N65M5

Schottky Diode: Infineon 600V 16A IDH16S60C



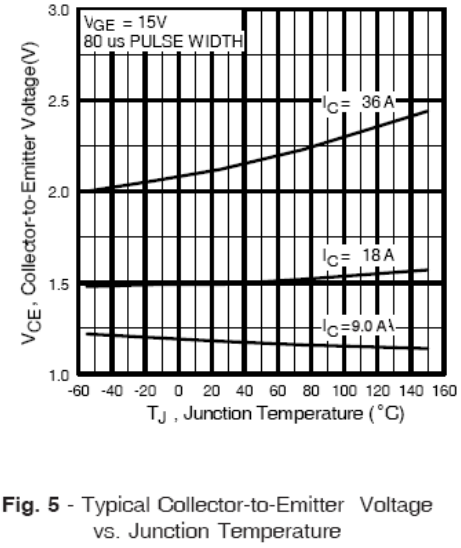
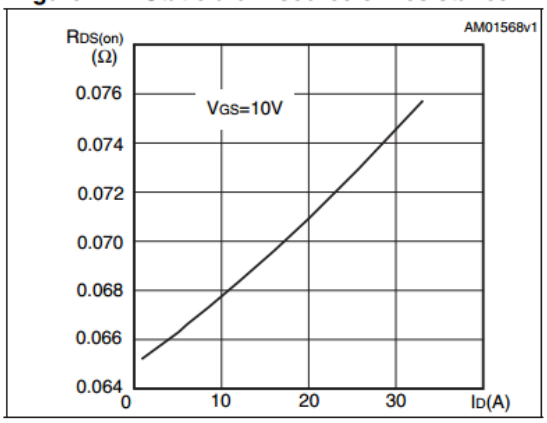


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

Figure Nº 35:IGBT$(V_{CE})_{SAT}$ drop vs. Collector Current w/ temperature considerations (AUIRG4BC30S-S).



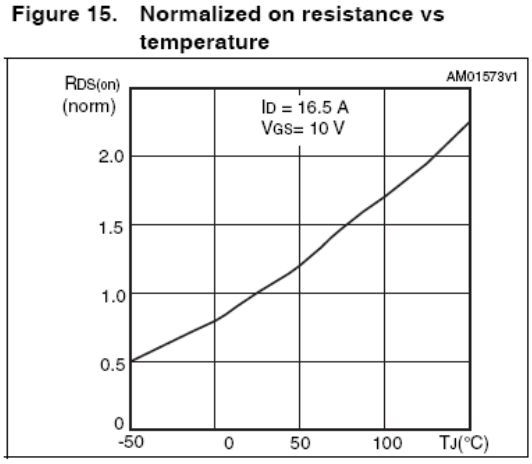


Figure Nº 36: Mosfet $(R_{DS})_{ON}$characteristic w/ temperature considerations (STP42N65M5).

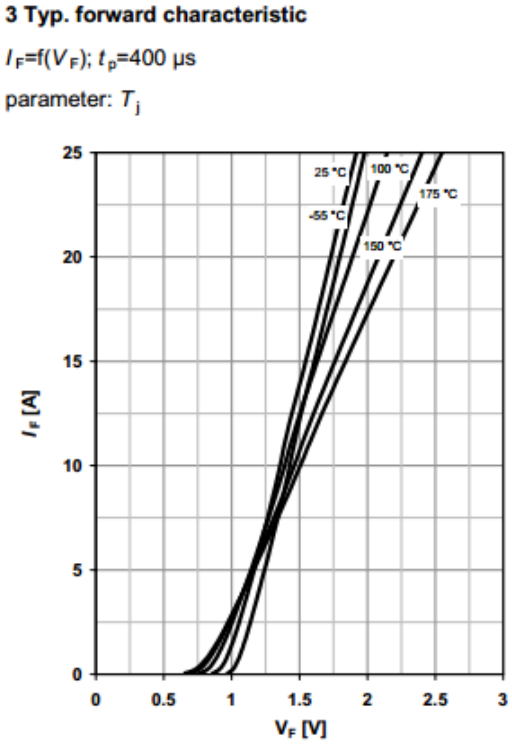


Figure Nº 37: Schottky Diode (V_F)characteristic (IDH16S60C).

Conduction losses has been estimated assuming four different current values and two different junction temperature $T_j = 100°C$ & $T_j = 75°C$, for 5, 10, 20 and 30A in order to verify the difference in terms of conduction losses, results are reported in the following tables:

Table Nº 1: Conduction voltage drops and on-resistance, temperature compensated at $T_j = 100°C$ with different switched currents according to figures 36 to 38.

-	5A	10A	20A	30A
IGBT - $(V_{CE})_{SAT}$	1,013V	1,1625V	1,528V	1,975V
MOSFET - $(R_{DS})_{ON}$	0,1139 Ω	0,1148 Ω	0,1207 Ω	0,1275 Ω
Schottky (V_F)	1,1V	1,2V	1,3V	1,6V

Table Nº 2: Conduction voltage drops and on-resistance, temperature compensated at $T_j = 75°C$ with different conducted current according to figures 36 to 38.

-	5A	10A	20A	30A
IGBT - $(V_{CE})_{SAT}$	1,025V	1,175V	1,5V	1,917V
MOSFET - $(R_{DS})_{ON}$	0,0938 Ω	0,0945 Ω	0,0994 Ω	0,105 Ω
Schottky (V_F)	1,1V	1,2V	1,3V	1,6V

Table Nº 3: ($\boldsymbol{V * I}$) or ($\boldsymbol{I^2 * R}$), MOSFET and Schottky Diode, $\boldsymbol{T_j = 75°C}$.

$\boldsymbol{P_{COND}}$ **[W]**	**IGBT**	**MOSFET**	**Schottky diode**
5A	5,125	2,35	5,5
10A	11,75	9,45	12
20A	30	39,76	26
30A	57,51	94,5	48

Table Nº 4:($\boldsymbol{V * I}$) or ($\boldsymbol{I^2 * R}$) IGBT, MOSFET and Schottky Diode, $\boldsymbol{T_j = 100°C}$.

$\boldsymbol{P_{COND}}$ **[W]**	**IGBT**	**MOSFET**	**Schottky diode**
5A	5,065	2,85	5,5
10A	11,63	11,48	12
20A	30,56	48,28	26
30A	59,25	114,75	48

The power product ($V * I$) or ($I^2 * R$)according to the case isrepresentative of the power dissipated in conduction, which is a leg duty cycle function, but this factor gives us an idea of the losses with similar duty cycles.

Is obvious the Mosfet losses will be greater conducting higher currents according to the calculations, but with low currents are always lower than IGBT and Schottky diode even the half of the losses factor than both other components in overall conduction losses are barely equal but commutation losses can be improved using mosfets caused by the high dynamic behaviour.

2.2 Components Cost

Passing form four components on the SAIL to two components for the 2-Mosfet IL, represent obviously a reduction of the number of components which will represent a cost reduction, but this fact can't be affirmed for every single case, because the components choice depends of the application and the project budget itself. Mosfet ON-resistance is inversely proportional to the component cost, treatment and materials should be spent to reach a reduction of the ON-resistance$(R_{DS})_{ON}$.

Considering this fact and the electrical conduction characteristic shown before is possible to say that reducing the number of components taking advantage of the Mosfets lower conduction voltage drop, in most cases will lead to a cost reduction for every single inverter leg.

2.3 Solution Approach

In the final part of Chapter I were exposed the dynamical problems linked to the 2-Mosfet Inverter Leg, the non linear output capacitance leads to EMI problem if hard-switching is implemented so the solution until now was slowing down the drive increasing the commutation losses, into the next analysis one solution is proposed reduce the Mosfet output capacitance effects.

First of all is important remember the output capacitance characteristic, for this analysis the Mosfet STP42N65M5 will be used so the waveform has been already introduced, in the following figure the output capacitance is reported from the component datasheet, also results taken from previous experiments [1] done in the Politecnico di Torino are reported in figure 39 considering the charge amount (Coulomb) necessary to charge the output capacitance for each Mosfets Turn-OFF with no load, in other words represents the leg total charge variation along the voltage in no load commutation.

Figure 12. Capacitance variations

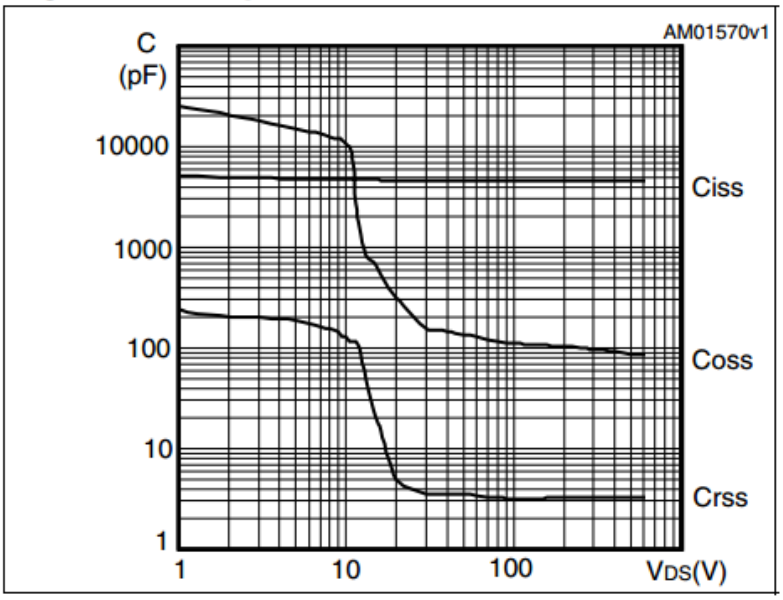


Figure Nº 38: Mosfet output capacitance (C_{oss}) (STP42N65M5).

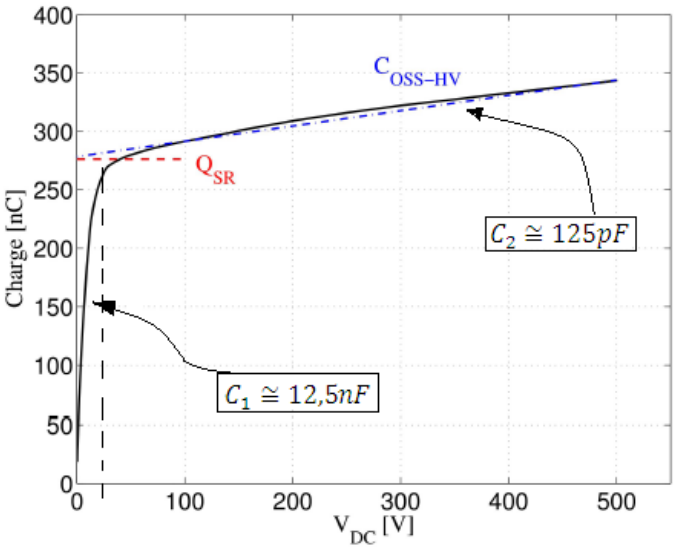


Figure Nº 39: Total leg charge for STP42N65M5.

A simple model can be done dividing the graph shown in figure 39 in two different approximately linear pieces and then calculate two different capacitance values, from 0V to 20V the resulting capacitance is $C_1 \cong 12{,}5nF$ and for the second part of the graph from 20V to 500V is possible to approximate to $C_2 \cong 125pF$. These values are coherent with the C_{OSS} available characteristic given by the datasheet reported in figure 38.

2.4 The Pulsed Active Desaturation

The solution here proposed follows the simple consideration of the non-linear charge function, reported in figure 39. This charge is stored for very low voltage drop and the resulting commutation process appears analogous to the "Desaturation" phenomenon of older bipolar devices. However in this case there's no loss in the desaturating device, behaving like a reactive non-linear capacitor, while the energy loss in induced in the turning ON switch (TR) due to high voltage commutation.

The basic concept is to supply this charge from a very low voltage source, instead from heavily higher DC-link voltage. The feasibility of the concept is related to the availability of such low-voltage source for each switching device. The solution is to provide a pulsed active application of the low voltage to the drain of the switching device every time is switched OFF, in order to supply such "desaturation charge" as much as possible but from the low voltage source: this is the Pulsed Active Desaturation.

The turn-ON commutation has two phenomena together interacting simultaneously, in first place the body diode reverse recovery of the turning-OFF switch (SR) and then non linear leg capacitance, so the analysis will be separated

in applying two different Pulsed Active low voltages according to the related phenomenon in order to complete each stage of the storage separately. The first one shall be done with a very low voltage when the body diode reverse recovery takes place: this will be named **Pulsed Active Storage Recovery, PASR** in the followings; while the second one can be completed with a slightly higher voltageproviding the charge necessary to complete the storage related to the non linear leg capacitance: this second stage will be named **Pulsed Active Capacitance Resonance, PACR** in the followings (motivated by the actual implementation).

2.5 The easiest PASR and PACR functional scheme

The easiest realization of the PASR and PACR concept is to apply the additional voltage supply, which is referred to the source, to the drain by means of a low voltage switch and a high-voltage diode. This is reported in figure 40 (referred only to the PASR), where the added switch is a P-Mosfet to easy command from the driving circuit. The command of the additional switch will be given by the output stage of the gate driver, turning it off immediately at the power switch turn-on, avoiding unwanted consumption from the additional supply. Let's point-out that the solution described above dissipates power from the PASR supply while charge is being provided to the power Mosfet.

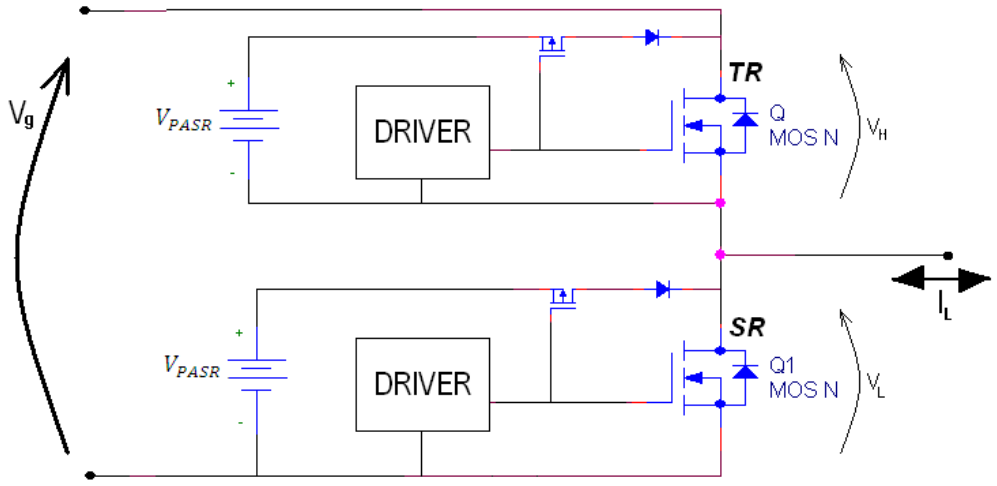


Figure Nº 40: Schematic structure of the Dissipative PASR.

In order to illustrate both Desaturation systems figure 41 is used, highlighting two different voltage generators connected to the power mosfet drain separately using the same configuration explained previously. PACR and PASR shouldn't start its action simultaneously, the PACR mosfet should be Turned-ON

after the PASR has done the first storage charge delivery, this is the reason why appears the time t_{PACR} meaning that PACR should wait before being turned ON.

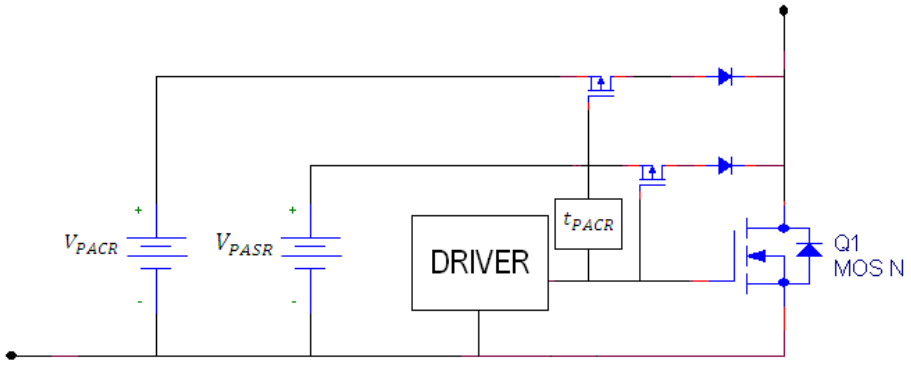


Figure Nº 41: Schematic structure of the Dissipative PASR and PACR.

2.6 Actual implemented PASR and PACR principles

Considering the easiest PASR and PACR implementation dissipates power from additional suppliers, a different scheme is proposed taking advantage of the system operation, in the followings principles and basic ideas of the actually implemented desaturating system will be shown.

2.6.1 PASR implementation principles

The next analysis is done considering the circuit actually used, partially illustrated in figure 42 where is possible to note that there's only one voltage supply and a transformer is used to supply the PASR voltage. Both desaturation systems have in series an inductance as a consequence of using transformer; this will lead to a still dissipative operation by PASR immediately explained.

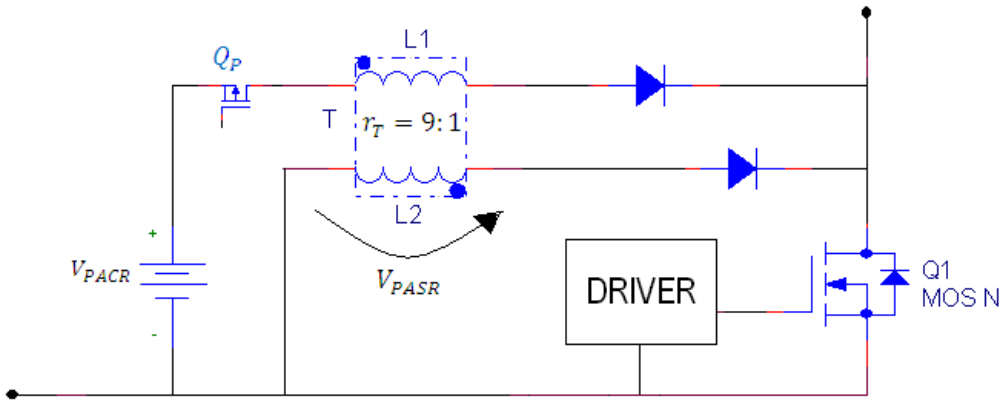


Figure Nº 42: Schematic structure of the implemented PASR and PACR.

When Q_P mosfet is turned ON the primary voltage equals the V_{PACR} voltageand according to the transformation ratio V_{PASR} will take a positive value, this fact produces a current flow coming from the load into the power mosfet drain and returning to the load (remembering the leg is it freewheeling state), in this way the reverse recovery of the body diode will be supplied by the PASR. The setup is realized with $V_{PACR} = 60V$ so transformer secondary voltage must be $V_{PASR} = 6{,}66V$ which to force the storage charge is enough. The voltage drop across the series diode (approx. 1V) reduces the effectiveness of the PASR because of the very low voltage supplied by the PASR.

The power dissipation by this method is not reduced, dominated by the secondary inductance dynamic which initially is discharged and when Q_P mosfet is turned ON start the transition with a low forcing voltage; the lower the inductance is, the lower will be power dissipation into the PASR, because the time in which the storage charge is supplied decrease.

To continue the analysis is important to highlight the characteristics of the transformer used, it is formed by two coils with a reduced coupling factor and a saturable core which allows having two different primary and secondary inductance values, this fact will be useful for the PACR stage, electrical characteristic of the saturable inductance is shown in figure 43.

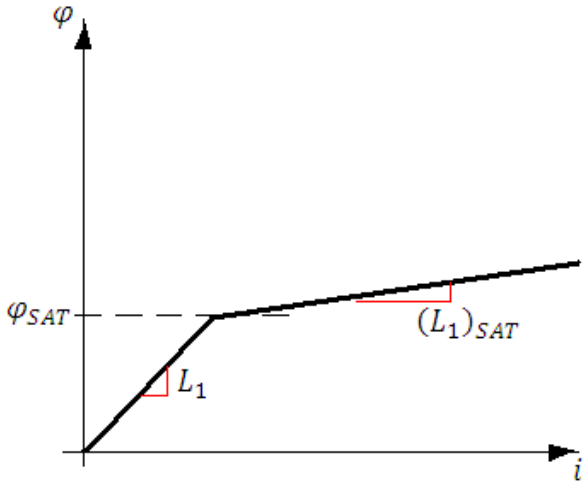


Figure Nº 43: Primary inductance characteristic.

When flux inside the core (φ) arrives to a certain value (φ_{SAT}) the primary inductance value will change becoming smaller ($(L_1)_{SAT}$). Once the inductance commutates to it smaller value storage energy is still supplied by the secondary inductance but major quantity of charge has been already supplied. This inductance commutation phenomenon is useful for the PACR stage immediately explained.

2.6.2 PACR implementation principles

This stage was named as Pulsed Active Capacitance resonance motivated by the resonant phenomenon which allows this second stage to have place. The order of events until the inductance saturation will be sequenced to a better understanding continuing with the successive stages: the body diode reverse recovery charge is supplied by the PASR stage from the moment when Q_P mosfet is turned ON, after certain time is elapsed the flux inside the core increase enough to saturate the core producing an inductance commutation, storage charge is still supplied to the leg capacitance increasing SR drain source voltage, when this voltage arrives over the 50V the leg capacitance became smaller as previously noted (see figure 39).

PACR stage will have place when leg capacitance commutates to it (smaller) linear value (C_2), the resonance will be between the linear leg capacitance ($(C_{lin})_{LEG} = C_2$) (for C_2 value see fig.39) and the saturated primary inductance ($(L_1)_{SAT}$) as shown in figure 43, and this phenomenon will supply the remaining charge useful to complete the SR Turn-OFF.

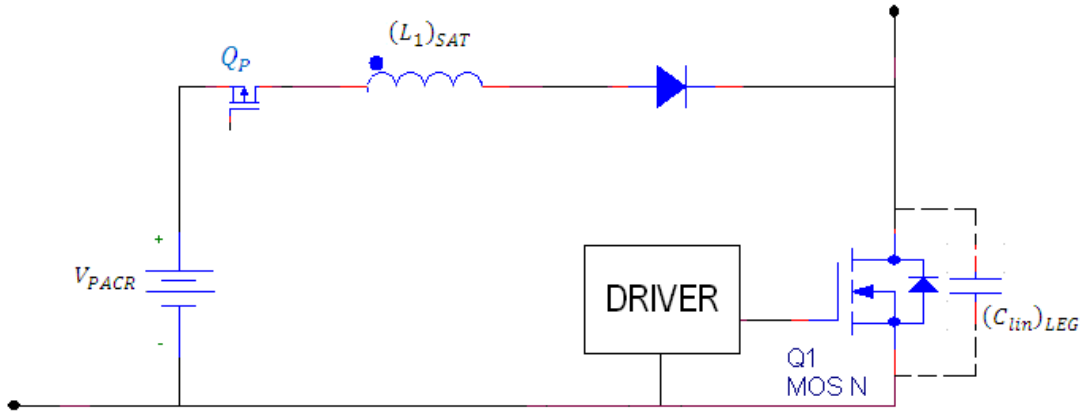


Figure Nº 44: Resonant circuit for PACR phase.

Is important to note that resonance will not only supply the necessary charge to open the SR mosfet but also will increase the $((v_{DS})_{SR})$ to a voltage higher than V_{PACR}, this voltage increase and the resonance frequency can be calculated with the next equations:

$$\Delta V = \sqrt{\frac{(L_1)_{SAT}}{(C_{lin})_{LEG}}} * I \qquad (12)$$

$$f_{PACR} = \frac{1}{2\pi * \sqrt{(L_1)_{SAT} * (C_{lin})_{LEG}}} \qquad (13)$$

Finally, once concepts are understood is important to note the second advantage of the resonance, while $(v_{DS})_{SR}$ is increasing the complementary voltage is decreasing this means the drain-source voltage across the TR allowing to make a turn-ON not only without overcurrent problems that initially carried the leg to EMI problems but with a reduced drain-source voltage, reducing losses by commutation. This fact leads to a different problem, the need of having a driver capable to recognizing the reduction of the drain source voltage and command the Turn-ON at the minimum voltage.

To illustrate all the Desaturation process fig. 45 is useful to give an idea of the concepts until now exposed, concentrating the process and pointing each desaturation stage as PASR and PACR, and also highlightingin a graphical way the need of the driver smartness.

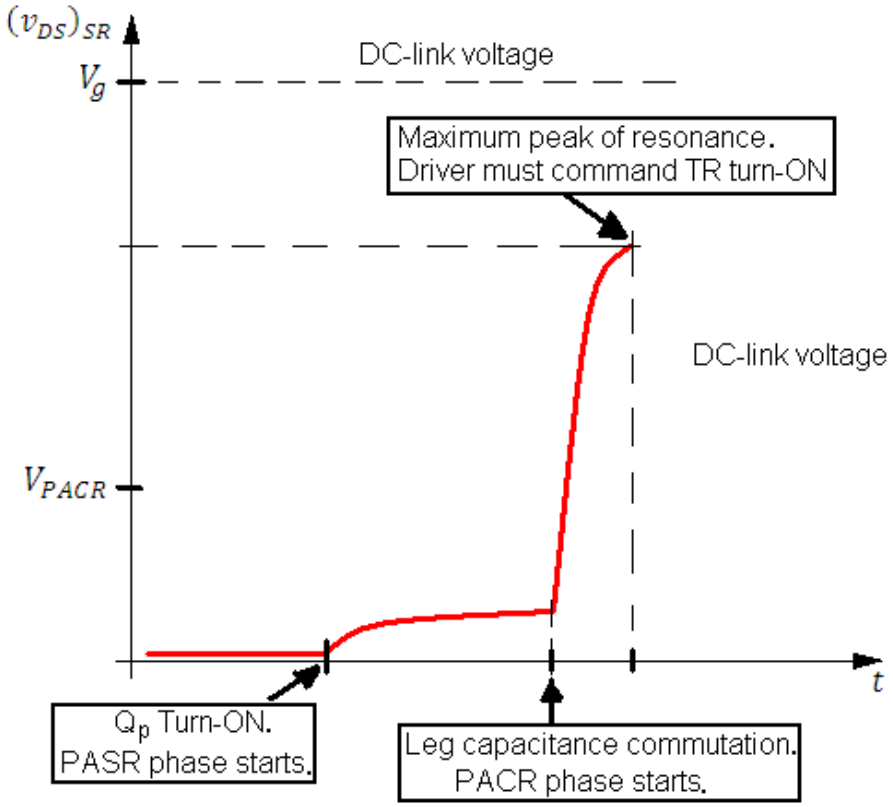


Figure Nº 45: Desaturation process highlighting inflection points.

2.7 Turn-On Consequences

In the previous chapter problems linked to the hard-switching commutation on 2-mosfet inverter leg were explained, and the conclusion was to slow down the driver in order to avoid the EMI problems generated by the capacitance commutations, increasing the commutation losses. The implementation of the Pulse Active Desaturation stages leads not only to the possibility of realizing hard-switching over the leg once the desaturation is finished but also to reduce the Turn-ON losses on the TR mosfet, because the voltage transition shall be finished with only a residual voltage and not with the full DC-link voltage when current transition is finished.

2.8 Turn-OFF Consequences

The turn-OFF of the TR mosfet is not affected by the implementation of the desaturation system, but some consideration must be done in order to guarantee full Electromagnetic Compatibility and autoinmunity when large currentsshould be interdicted.

2.9 Snubber and Clamped implementation

Taking into account that Turn-ON commutations are already dominated, desaturation system will be modified in order to fully dominate Turn-OFF commutations, when large currents must be commutated by mosfets, just like previous analysis turn-ON and turn-OFF commutation are referred to the TR mosfet.

Opening the TR mosfet produces a $^{dv}/_{dt}$ variation governed by leg capacitance, commutating large current higher voltage variations are produced and those variations should be controlled, the circuit shown in figure 46 is a partial modification of the PAD to accomplish this objective (Note: PASR and PACR remains identically, present "modifications" are additional).

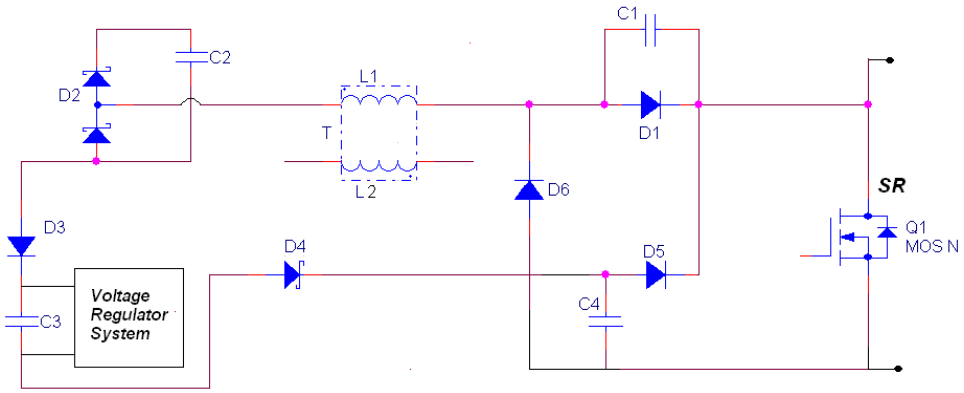


Figure Nº 46: Snubber and Clamped Circuit for Turn-on domination.

For the shown circuits each component function is analyzed in order to illustrate the implemented solutions to reduce voltage steep slopes on turn-OFF, two solutions has been adopted, the first one is a **Snubber** and acts with higher $(v_{DS})_{SR}$ being used to reduce voltage slope from certain initial voltage level. The second solution acts when the voltage transition is almost finished in order to reduce if possible the overvoltage across the turning-on mosfet, and will be called as **Clamped**.

Snubber and Clamped capacitors has to be prepared before the turn-OFF commutation to the desired initial voltage level when the turn-OFF commutation starts, this is done in "recharge stage" which is accomplished just after the turn-ON. In other words, when the PASR and PACR supply the storage charge to the SR, TR mosfet is Turned-ON and then recharge stage of Snubber and Clamped capacitors start.

2.9.1 Snubber and Clamped recharge

When TR is ON, the $(v_{DS})_{SR}$ barely equals the DC-link voltage (V_g) keeping reverse biased the body diode with the SR mosfet open there's a current path from capacitor C1 passing through L1, D2, C2, D3, C3, D4 and finally C4 returning back to DC-link, this current path generates an impulsive current which charges the inductance, once the inductance is totally charged the impulsive current arrives to it maximum value. Then inductance discharge takes place with the D6 as a freewheeling diode, which allows the current circulation from the inductance through the capacitors C2, C3 and C4 charging them to a certain voltage level, simultaneously reset C1 condenser.

One important consideration shall be done about C3 capacitor which is depicted with a voltage regulator system; this allows regulating capacitor voltage level at desired value, for the active stage of the Snubber.

Summarizing the analysis, in the recharge stage the inductance accumulates energy which will be supplied to C2, C3 and C4 capacitor thanks to the freewheeling diode, while C2 condenser is reset. The voltage level reached by C2, C3 and C4 will determinates the initial voltage level given to D1 anode or what is the same, to C1 left terminal.

2.9.2 Active stage of the Snubber and Clamped and consequences

When turn-OFF is commanded, Snubber capacitor initial voltage defines the performance of the snubber, is C3 regulation system discharge it to its minimum regulated level the Snubber capacitor will act reducing $^{dv}/_{dt}$.

On the other hand, if C3 regulation system does not reduce its voltage level keeping it at the maximum regulated value, Snubber will not interact with the leg which implies that $^{dv}/_{dt}$ is dominated by mosfet dynamic.

In the final part of voltage transition when $(v_{DS})_{SR}$ is lower than Clamped capacitor voltage, all the stored charge is supplied to the load from capacitor reducing overvoltage and damping the waveform after SR turn-ON. This overvoltage reduction is proportional to the clamped voltage, so recharge stage will define the impact of the clamped.

2.10 The 2-Mosfet I.L. General scheme

After the overall analysis over the different phenomenon related to the 2-Mosfet Inverter Leg and the proposed solutions to make possible commutations is important to resume all the analysis to fix the concepts. As seen before the major commutation issues became when a Mosfet is used as SR caused by body diode

conduction and must change its conduction state passing from ON to OFF, even when to body diode does not conduct all the current, reverse recovery takes place; this commutation motivates the PASR and PACR implementation to control the Turn-ON (always referred to the TR mosfet). Once this objective is reached there is a freedom degree which allows also to control the Turn-OFF commutation at large currents, which is done with the Snubber and Clamped circuits modifying the desaturation circuit. The resulting circuit used to assist commutations will be called in the followings as **Ideal Hard Commutation (IHC)**.

Until now each inverter leg mosfet has been named differently, as SR and TR according to its conduction state assuming specific performance to each mosfet but in the I.L both mosfet will perform as TR or SR as well according to the load requirements (always as complement between each other) so IHC will be implemented for both mosfets as follows in figure 47.

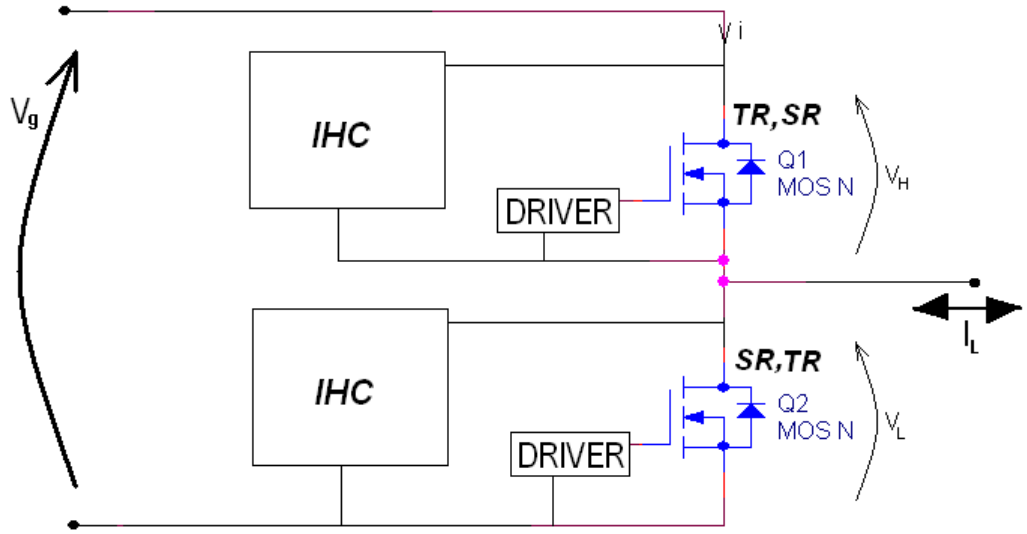


Figure Nº 47:2-Mosfet Inverter Leg with commutation auxiliary system.

CHAPTER III

TEST BENCH THEORY

3.1 H-bridge Structure

In order to verify experimentally the 2-Mosfet I.L advantages a system which allows to measure power losses by conduction and commutations has to be implemented, some working conditions has to be considered to guarantee the correct measurement of the variables involved. So the desired structure to test the system has the objective to allow power losses quantification having a stable operation mode, which is able to not disturb the single inverter leg performance allowing verifying expected theoretical results.

Is important to highlight, high efficiency leg inverter is the DUT (device under test) of the present test bench, so every experimental condition has to be specially thought under this hypothesis. The principal objective of the test bench is to quantify commutation power losses in order to establish several conclusions.

Looking forward to reach the objective, H bridge configuration formed by two inverter legs (reported in figure 47) allows to control the current direction having two complementary structures connected supplied by an unipolar DC-link voltage (V_g), two situations must be guaranteed:

- Low input voltage ripple (Δv_C)
- Low output current ripple (Δi_L)

Avoiding output and input ripple the single I.L. structure will work in stable conditions for sure, this implies with a constant commutated voltage level and a constant commutated current, so the Device Under Test (DUT) became only the structure and unwanted phenomenon in the supplier or the load may not occur because those work in a constant manner during H-bridge performance.

To reach first of the objectives input condensers value was raised until capacitance that reduce as much as possible input voltage ripple, these capacitors where placed nearby the H-bridge in order to reduce the connection inductance and optimize the dynamic.

Equally output ripple reduction is reached by increasing the output reactive phenomenon, in other words using a Pure Inductive Load which implies a large dynamic to accumulate or lose energy. According to the type of modulation used

to control the H-bridge low output dynamic will lead to highly stable output current.

Implemented type of modulation

In order to maintain constant output current, both Inverter Legs are commanded in ”first harmonic cancelled bipolar modulation”, in other words impulsive currents are produced with a large freewheeling stage taking advantage of the wide output current dynamic reached with pure inductive load. This fact is illustrated in figure 48 showing the pulsed voltage waveform expected and the constant output current.

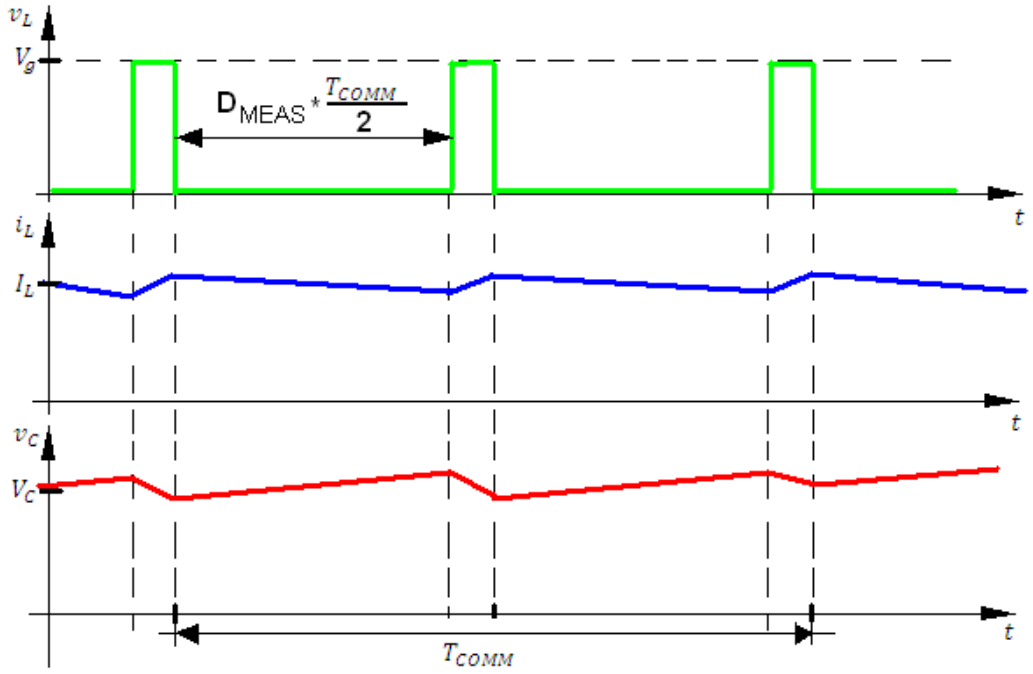


Figure Nº 48: Output and input used waveform for the test bench

3.2 Test Bench Set-up

The effects of implementing IHC with the 2-mosfet leg inverter will be qualified and quantified experimentally; the quantification will be made in terms of commutation efficiency where commutation losses should be indirectly measured. On the other hand effects qualification can be done with the output waveforms.

In order to measure qualitative and quantitative characteristic a laboratory set up is realized as shown in figure 49.

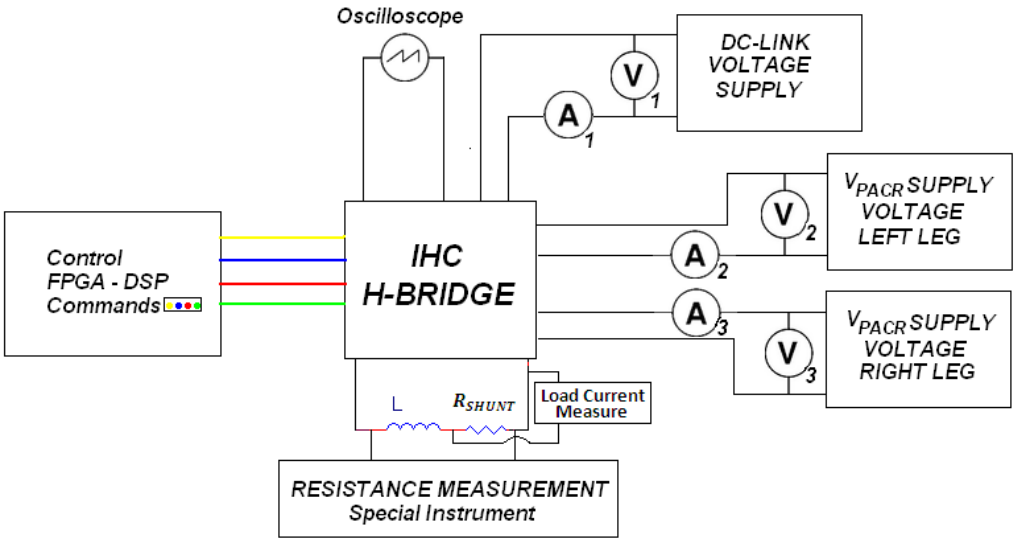


Figure Nº 49: Block diagram of the Laboratory Set-up

3.2.1 Inverter leg characteristics

Motivated by technical reason IHC will be implemented for one mosfet by leg and consequently mosfets will have specialized performance, the H-bridge is shown in figure 50, is important to note several technical aspects:

- Each power mosfet is implemented by 3 power mosfet in parallel for handle larger currents; figure 51 illustrates the left leg formed by 3 mosfets.
- For the left leg the SR mosfet will be the upper one so IHC is implemented between drain and source of this mosfet, also for the lower mosfet of the right leg which will be the one working as SR.

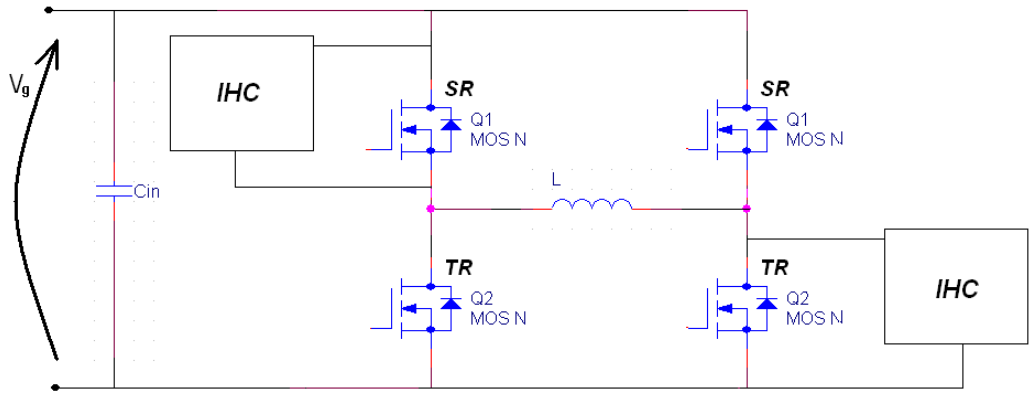


Figure Nº 50: H-bridge implemented with two mosfet inverter leg

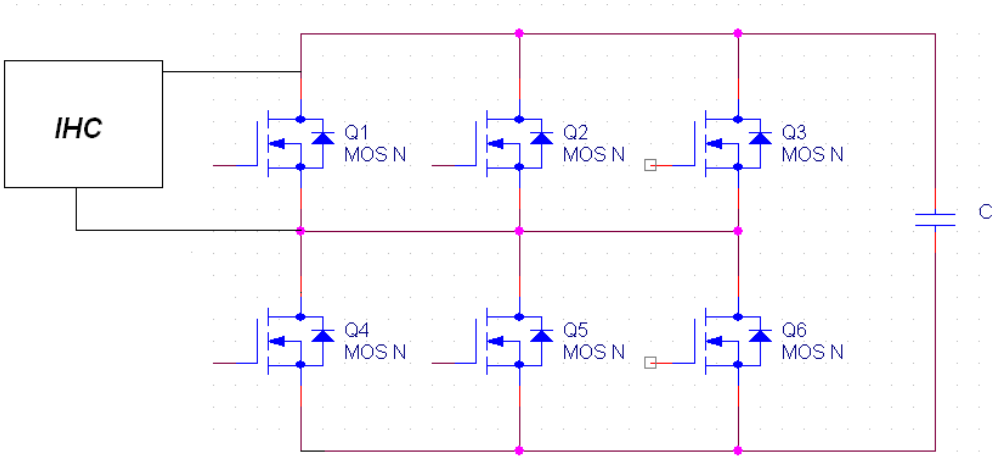


Figure Nº 51: Left leg showing how the leg is actually formed by 3 power mosfet in parallel.

Once technical aspects are clear about inverter legs configuration is important to turn back to the test set-up (figure 49) where are shown all the measurement instrument and equipment used to quantify total losses, conduction losses and qualify waveforms from oscilloscope. As specified initial in the present chapter the objective of the test bench is to quantify the total commutation losses in order to verify the theoretical assumptions done for the construction of a new inverter leg.

The Control of every single mosfet is done from a FPGA (Field-Programmable Gate Array) which generate commands useful to each mosfets, the setting of the parameters is done from a PC, this stage will be only commented because is not the objective of the present study.

3.3 Total Losses Calculation

In typical converter configurations the total energy used by the converter and the load is supplied by the DC-Link voltage supply and determinate the power supplied by the generator will be the simple current-voltage multiplication. In this case there's not only the DC-Link voltage supply but also the IDH voltage supply from each leg, called V_{PACR} in figure 44.

So determinate the total energy given to the converter will be not only the voltage-current multiplication of the DC-link generator but also the current-voltage product of each IHC generator, as follows:

$$P_{TOT} = V_1 * I_1 + V_2 * I_2 + V_3 * I_3 \qquad (14)$$

The total power will be representative of the lost energy in commutations plus the lost energy by current conduction and since the load is purely inductive

power consumption will be almost zero, just the energy lost in the resistance of the wires; this load power consumption will be considered as lost power by current conduction.

So the total power supplied by the generators is equal to the power lost by commutations and by current conduction, as indicated by the following equation:

$$P_{TOT} = P_{COND} + P_{COMM} \qquad (15)$$

3.4 Conduction losses calculation

Having commutation efficiency as the present test bench objective put in front a problem, and this is calculation of power losses by current conduction. The main difficulty is to measure the resistance along the current path, because the current will be measure with known instruments. To solve this problem, a special instrument should be constructed in order to quantify experimentally under duty conditions the resistance of the current path.

3.4.1 Resistance Measurement Instrument

Based on modulation waveform an instrument has been design to measure the output voltage (v_L in figure 52) and knowing the load current (i_L) resistance can be calculated. As noted before, output voltage presents two different stages motivated by the modulation ("first harmonic cancelled bipolar modulation") the first one is an impulsive voltage used to keep constant output current and the second one is the freewheeling stage where resistance can be calculated because voltage is almost constant.

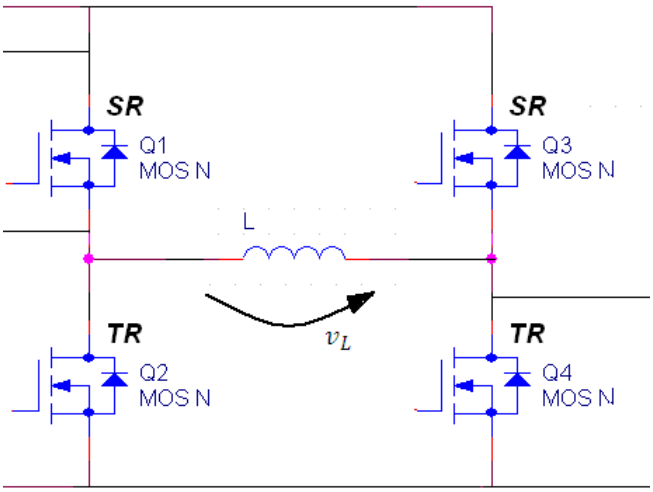


Figure Nº 52: Schematic output measured voltage

Schematic measure circuit is depicted in fig. 53, where is possible to see that when impulsive large voltage arrives to the instrument terminal, superior Schottky diode is in its conduction state and the measured voltage v_R equals the Schottky threshold voltage which is approximately $v_R = 500mV$ for a very short time, and then when freewheeling stage takes place the measured voltage is the output voltage because upper Schottky diode is reverse biased. To clarify how v_R is measured is enough to say that using a typical voltmeter allows to have an average value useful to proceed with the resistance estimation.

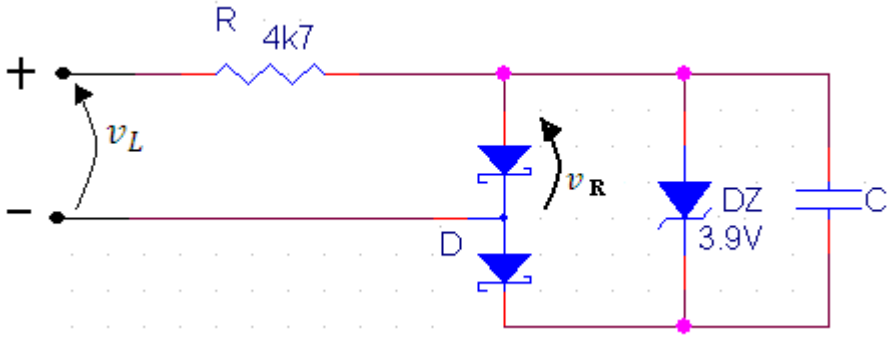


Figure Nº 53: Schematic resistance measurement circuit

With the conceptual performance of the measurement circuit, equation can be written in order to relate the measured voltage v_R with the conduction resistance as follows:

$$v_R = R_{ON} * I_L \quad => \quad R_{ON} = \frac{v_R}{I_L} \qquad (16)$$

$$\widetilde{v_R} = \frac{v_R + v_{SCK} * \frac{t_{SCK}}{T} + 0.6 * v_{SCK} * \frac{t_{PASR}}{T}}{D_{MEAS}} \qquad (17)$$

Measured voltage v_R should be compensated in order to correct measurement errors caused by the impulsive voltage level, as said before impulse voltage causes diode Schottky conduction for a certain time (t_{SCK}=t_{IMP}) where t_{IMP} is the time during impulsive voltage takes place, in other words is the time during H-bridge diagonal is used to generate impulsive current. The second compensation is made motivated by the PASR stage (pulsed active storage recovery) which as explained in Chapter II section 2.5.1 takes place for certain time before the Turn-ON of the TR Mosfet, so this initial voltage will bias directly the upper Schottky diode with a very-low voltage so voltage drop will be lower than threshold voltage (approx $v_{SCK} = 0.3V$).

Finally is important to note that corrections are done to decrease as much as possible measurement errors, the impulsive voltage will last around 100ns to 300ns when commutation frequency is 30 kHz, which implies that first correction

represents around 3‰ of the period, while the PASR will last around 900ns according to design approach what represents approximately 3% of the period. In conclusion error correction will only represent approx 3.3% of the effective time for measure by period, with low voltages variations (as v_{SCK} can be).

Once the measurement instrument concept and implementation is understood only remain the further compensation of the measured resistance which is based on add the inductance resistance ($R_{IND} = 12{,}7m\Omega$ according to a static measure done in laboratory) to the calculated resistance as this is also part of the loop.

$$(R_{ON})_{LOOP} = R_{on} + R_{IND} \tag{18}$$

$$(R_{ON})_{LOOP} = \frac{\widetilde{v_R}}{I_L} + R_{IND}m\Omega = \frac{\frac{v_R + v_{SCK}*\frac{t_{SCK}}{T} + 0.6*v_{SCK}*\frac{t_{PASR}}{T}}{D_{MEAS}}}{I_L} + R_{IND}m\Omega \tag{19}$$

At this point lost power by current conduction will be easily calculated as follows:

$$P_{COND} = {I_L}^2 * (R_{ON})_{LOOP} \tag{20}$$

One last comment will be necessary, as can be saw very special care was took in order to determinate with the minimum error as possible conduction current

3.5 Commutation losses calculation

Once total and conduction losses are determined commutation losses will be easily calculated by subtraction, but is important to note that very special care was took in order to determinate with the minimum error as possible the conduction resistance because the error of this measure will be highly impacting into the Commutation losses, which is a defining parameter on the commutation efficiency calculation.

$$P_{COMM} = P_{TOT} - P_{COND} \tag{21}$$

3.6 Commutation Losses per cent calculation

The per cent losses will be calculated for each inverter leg, so the commutation power losses should be divided by 2 times the commutation product (Switched Voltage times Switched Current), because P_{COMM} represents the total H-bridge commutation losses.

$$P_{COMM}[\%] = \frac{P_{COMM}}{2*V_g*I_L} \tag{22}$$

Being more precise further correction is done, taking into account that for the H-bridge left leg IHC voltage supply is not referenced to ground potential because the Desaturation System is referred to the source of the upper mosfet so every commutation moves the parasitic capacitance of the supplier transformer from the DC-link voltage to ground, producing a loss of energy equal to$(E_{IHC})_{LL}$ (Energy lost by the IHC in the left leg) and must be subtracted to the commutation losses because is an external phenomenon:

$$(E_{IHC})_{LL} = \frac{1}{2} * C_{Paras} * \left(V_g\right)^2 \Rightarrow (P_{IHC})_{LL} = (E_{IHC})_{LL} * f_{SW} \qquad (23)$$

So finally commutation per cent losses can be written as:

$$P_{COMM}[\%] = \frac{P_{COMM} - (P_{IHC})_{LL}}{2 * V_g * I_L} \qquad (24)$$

The commutation power losses are calculated considering all the linear and non-linear phenomena participating in each commutation for both inverter legs, this allows to quantify how efficient is the IHC system and also how efficient can be and inverter leg based in mosfet.

CHAPTER IV

DESING CONSIDERATION AND EXPERIMENTAL RESULTS

4.1 Design Stage

4.1.1 Electrical Circuits

Electrical design programs were used in order to realize inverter legs with IHC system, from the schematic circuits to the layout of printed boards corresponding to the PCB and drivers; particularly for the present study PSpice was used.

PSpice: CAPTURE, used for schematic circuit's project.

LAYOUT: used for layout's project.

Schematic circuits for power circuit realized with PSpice-Capture are shown as follows:

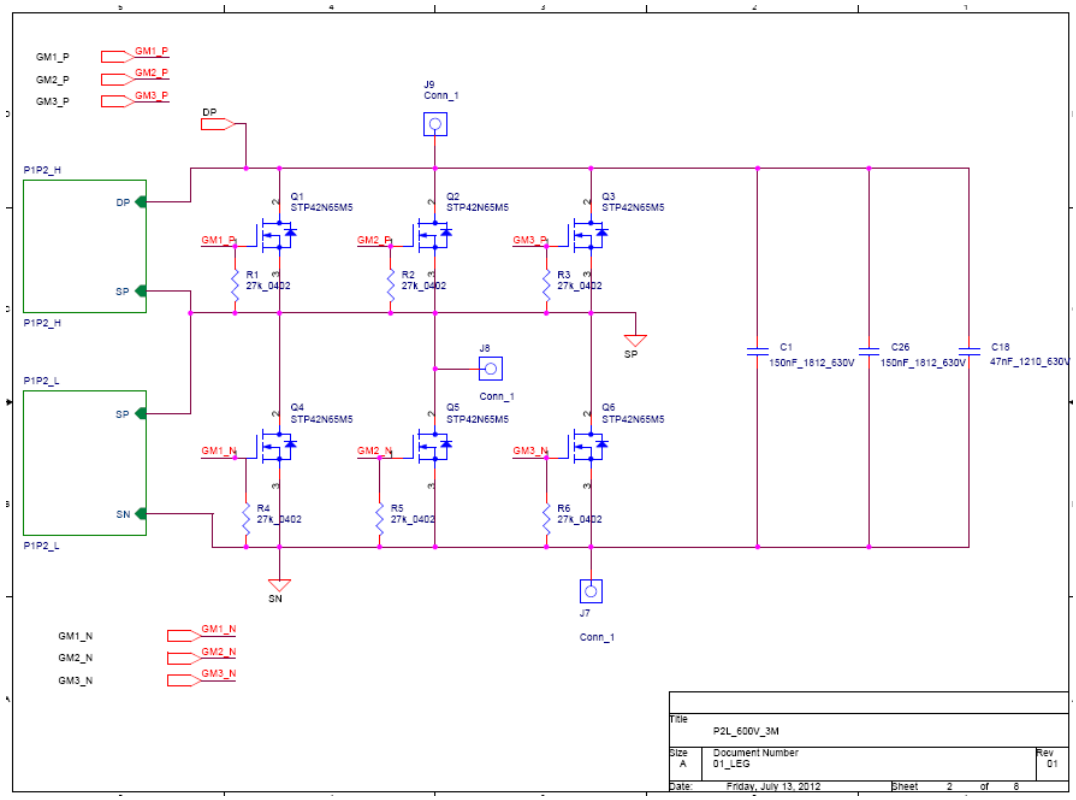


Figure Nº 54:2-Mosfet leg Schematic Circuit – PSpice-Capture

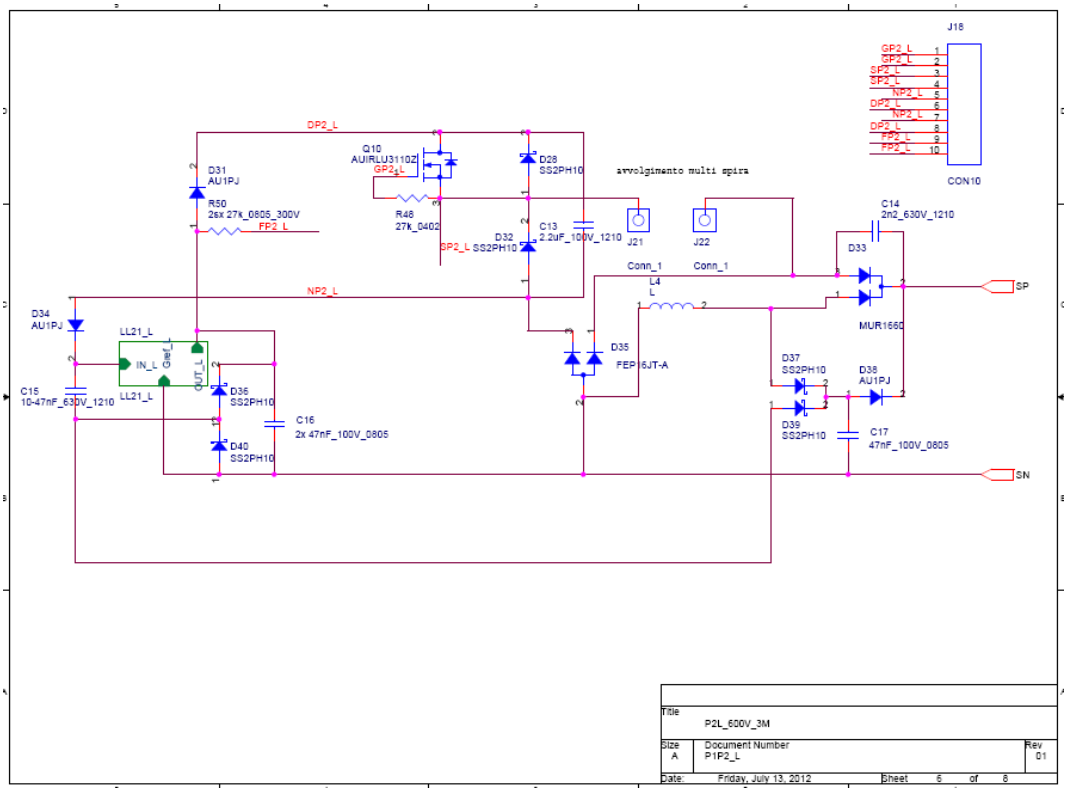


Figure Nº 55: Lower Mosfet IHC Schematic circuit – PSpice-Capture

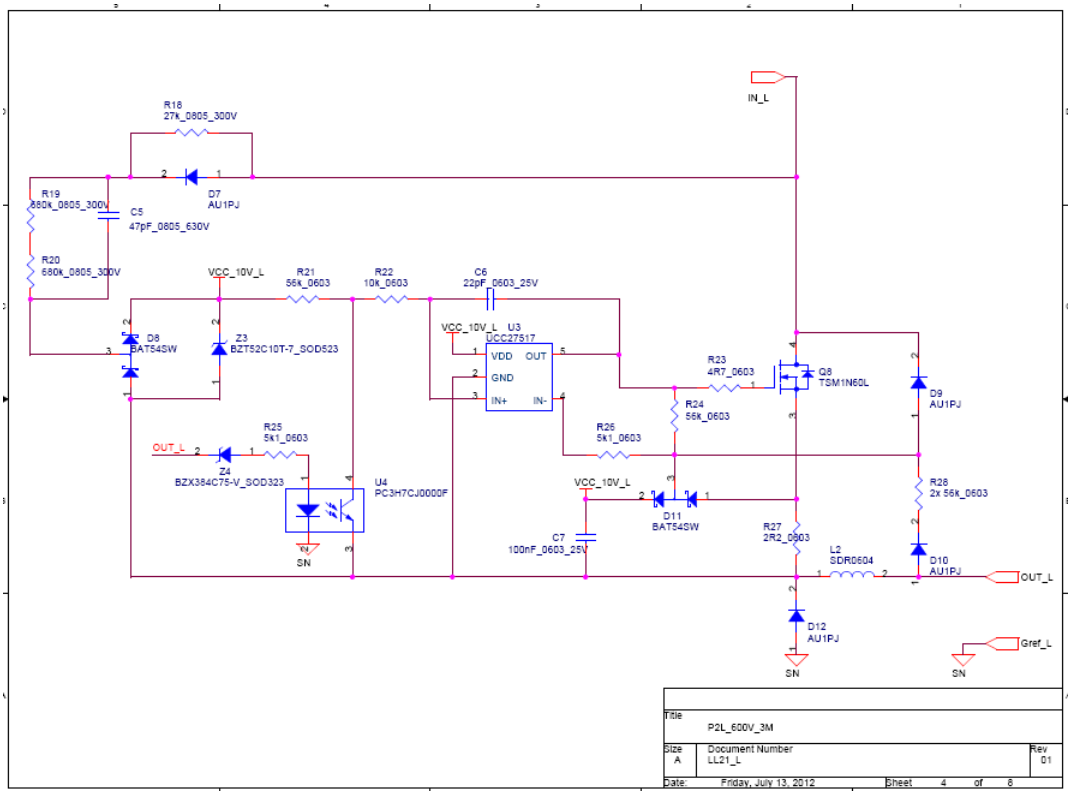


Figure Nº 56: Voltage regulator Schematic circuit – PSpice-Capture

4.1.2 Physical Assembly Considerations

Components were positioned in order to be compatible in physical assembly; in order to any possible physical problem SolidWorks program was used for designing. Both projects phases were done simultaneously, not only the electrical circuits but physical assembly simulation.

Some 3D system draws made with SolidWorks are shown in figures 57 and 58 with the aim of illustrate physically the system.

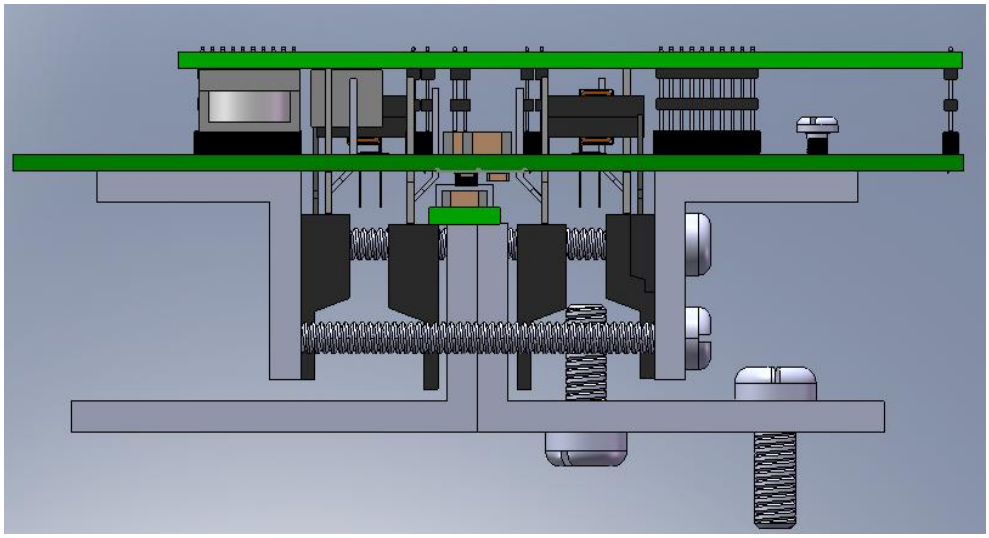


Figure Nº 57: Frontal view SolidWorks simulation H-bridge + driver

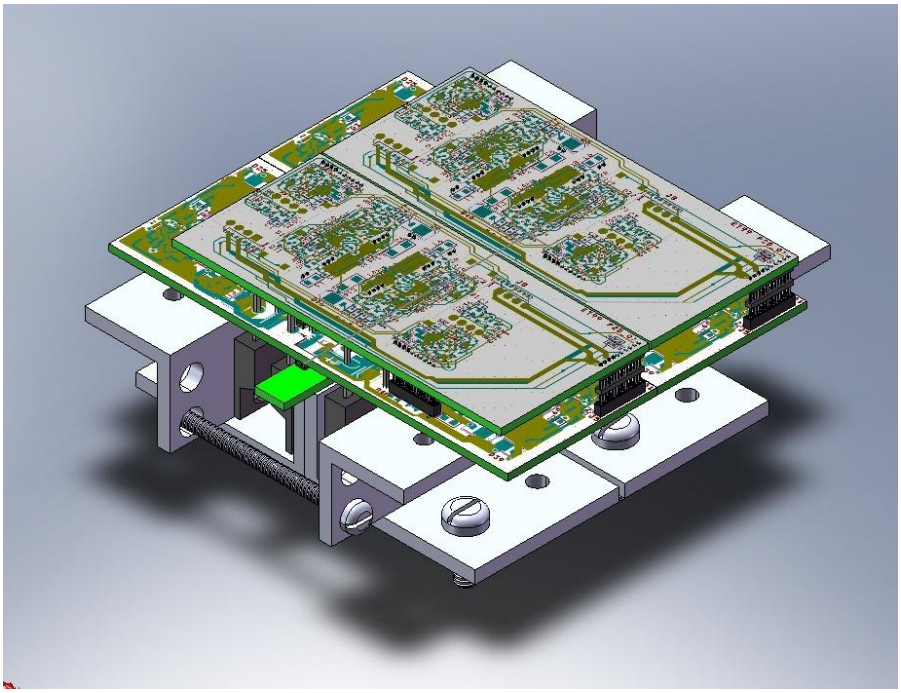


Figure Nº 58: Isometric view SolidWorks simulation H-bridge + driver

4.2 Experimental Results

4.2.1 Qualitative Analysis

Using the test bench set-up explained is Chapter III, Section 3.2 experimental results were obtained in order to verify qualitatively and quantitatively IHC structure performance and effectiveness.

Duty conditions are the followings:

- Switched voltage: $V_g = 400V$
- Switched Current I_L , is a variable in order to quantify commutation losses as a current function
- Switching frequency $f_{SW} = 30kHz$
- IHC voltage supply V_{PACR} for right and left leg $((V_{PACR})_H, (V_{PACR})_L)$ were controlled variables with the objective to improve the system efficiency but were contained between 60 and 75 V

In first place qualitative results were obtained evaluating each leg output voltage, following images shows output voltage with an $I_L = 20A$ switched current, useful to verify on each Turn-ON and Turn-OFF commutation the effects of IHC structure.

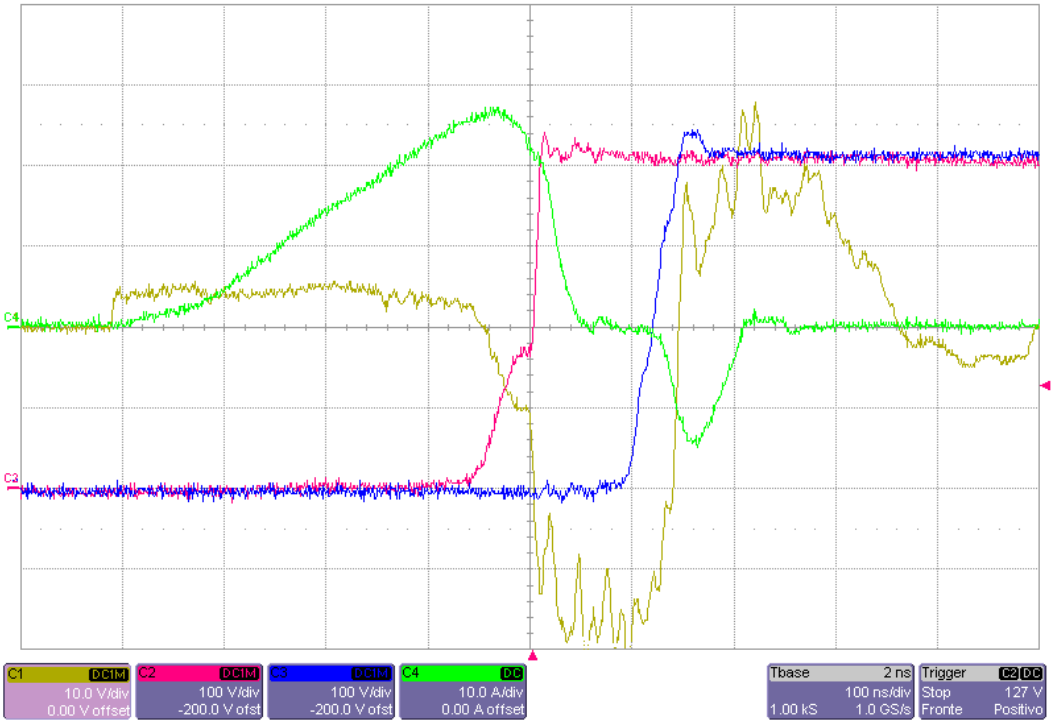


Figure Nº 59: Turn-ON and Turn-OFF commutation VSIL (Time scale: 100ns/div, voltage scale 100V/div).

Red Line: Turn-ON commutation right leg

Blue Line: Turn-OFF commutation left leg

Green Line: PACR primary coil current

Yellow line: PASR voltage

With Fig.59 is possible to see in first place how dominated commutations are, time scale is 100ns/div which indicates that voltage transitions are done in less than 50 ns in hard-commutation

In the followings Turn-ON commutation is described and analyzed in details.

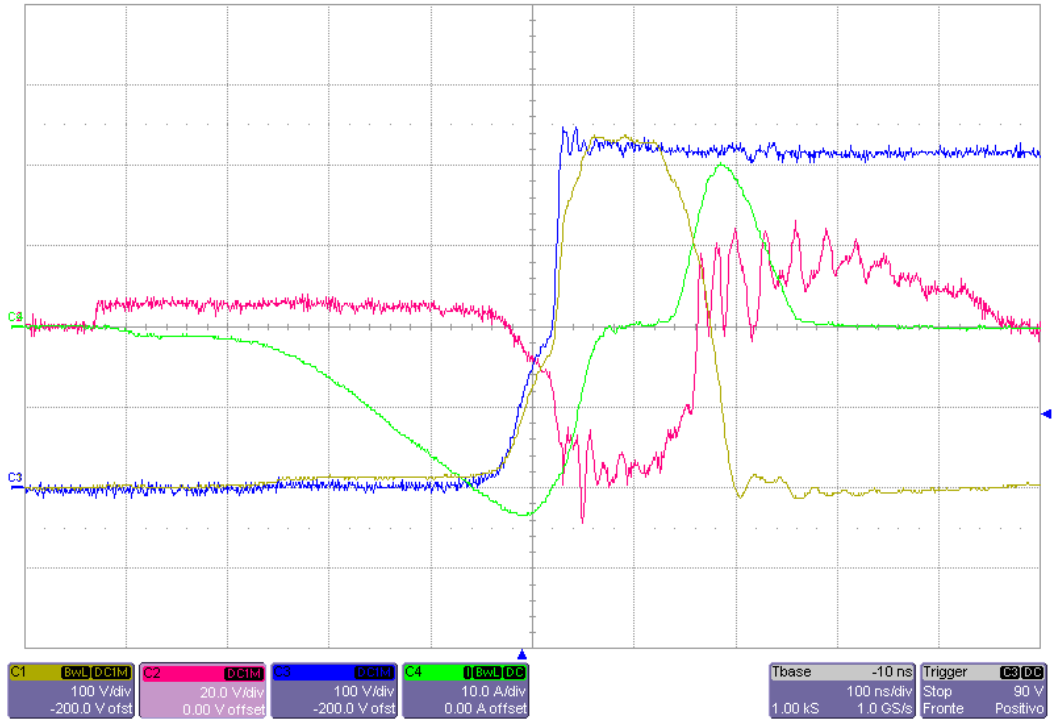


Figure Nº 60: Turn-ON commutation right leg (Time scale: 100ns/div, voltage scale 100V/div)

Red Line: PASR voltage (20V/div)

Blue Line: Turn-ON commutation right leg (100V/div)

Green Line: PACR primary coil current (Inverted) (10A/div)

Yellow line: PACR primary coil voltage (100V/div)

With red line is possible to see that PASR voltage 5V lasts around 400ns, the time to supply charge for body diode reverse recovery and large initial leg capacitance, the primary coil inductance current raise charging it with low slope and then change to a steep slope due to core saturation, after 400ns are passed resonance starts.

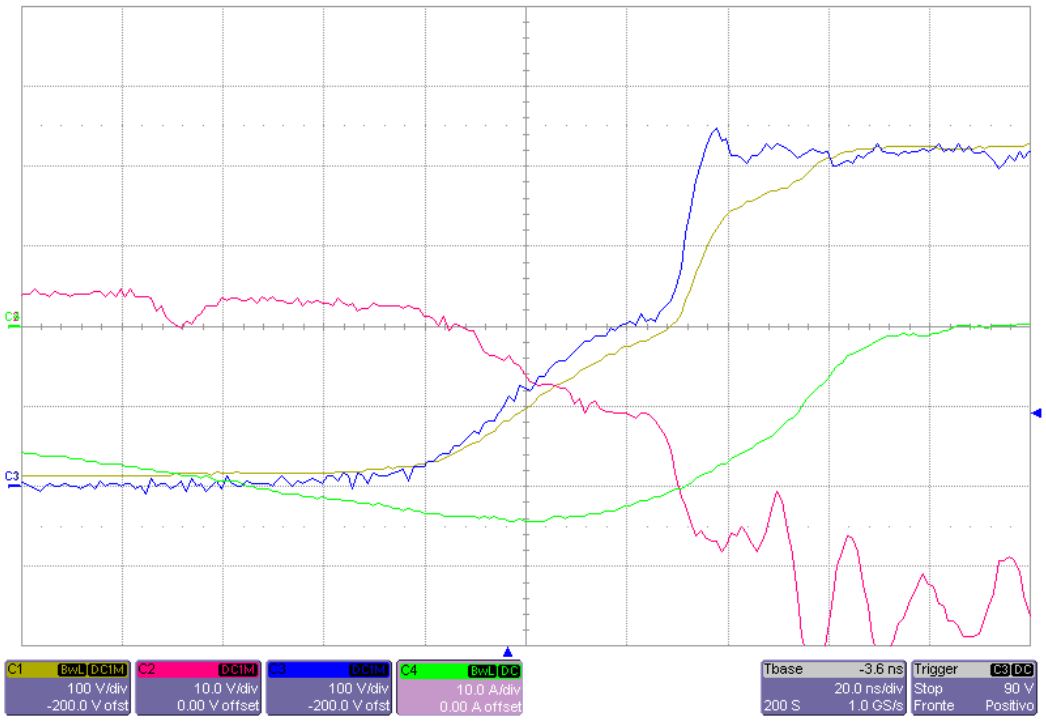


Figure Nº 61: PACR resonance zoom (Time scale: 20ns/div)

Red Line: PASR voltage (10V/div)

Blue Line: Turn-ON commutation right leg (100V/div)

Green Line: PACR primary coil current (Inverted) (10A/div)

Yellow line: PACR primary coil voltage (100V/div)

Resonance starts discharging the inductance while SR voltage is raising, reducing voltage across the TR mosfet, resonance half wave last around 40ns and then hard-switching is realized on the mosfet by driver when has minimum voltage of 200V approx, this fact lead to a turn-ON commutation with quasi-zero losses, and provide non linear charge to body diode externally reduces to zero overcurrent in the turning-ON mosfet.

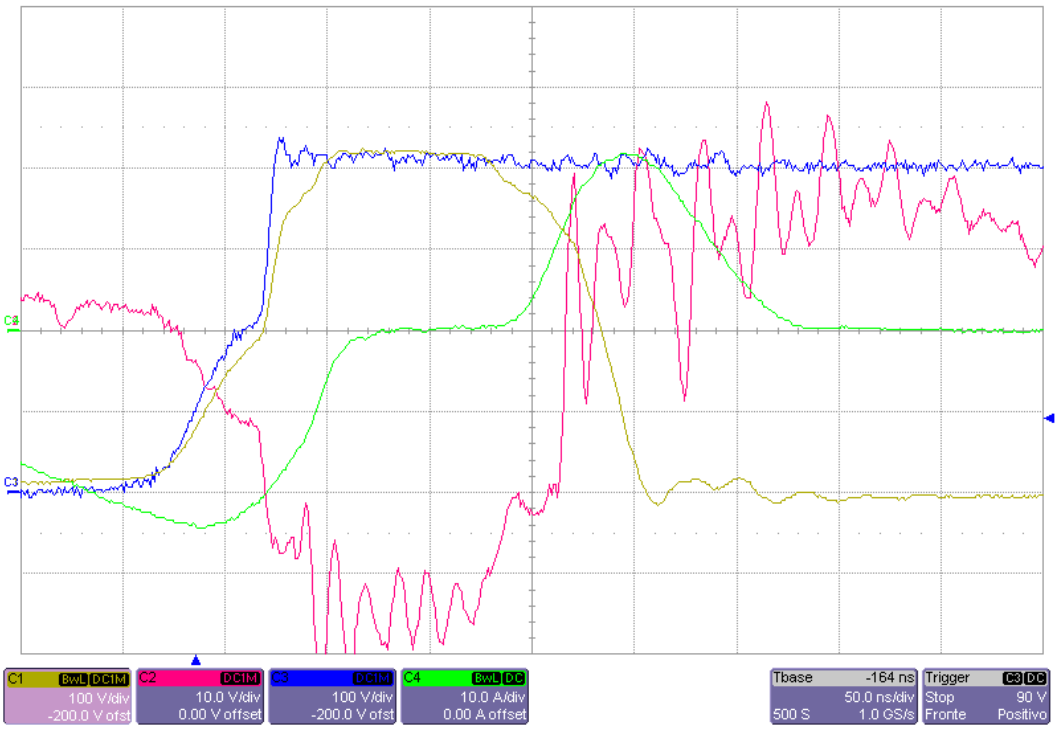


Figure Nº 62: Snubber and Clamped capacitor reset (Time scale: 50ns/div)

Red Line: PASR voltage (10V/div)

Blue Line: Turn-ON commutation right leg (100V/div)

Green Line: PACR primary coil current (Inverted) (10A/div)

Yellow line: PACR primary coil voltage (100V/div)

Just after turn-ON snubber and clamped recharge stage is realized, with a current into primary inductance in opposite direction desaturating and saturating transformer coil immediately until inductance is totally charged (maximum current is achieved), voltage in the primary coil goes together with DC-link until inductance is charged and then freewheeling diode acts moving the stored charge on the inductance into snubber and clamped capacitors in order to reset its voltage levels, when freewheeling starts primary coil voltage goes approx. to zero. After inductance current is null snubber and clamped capacitor are reset.

Next commutation is the turn-off, and is immediately analyzed:

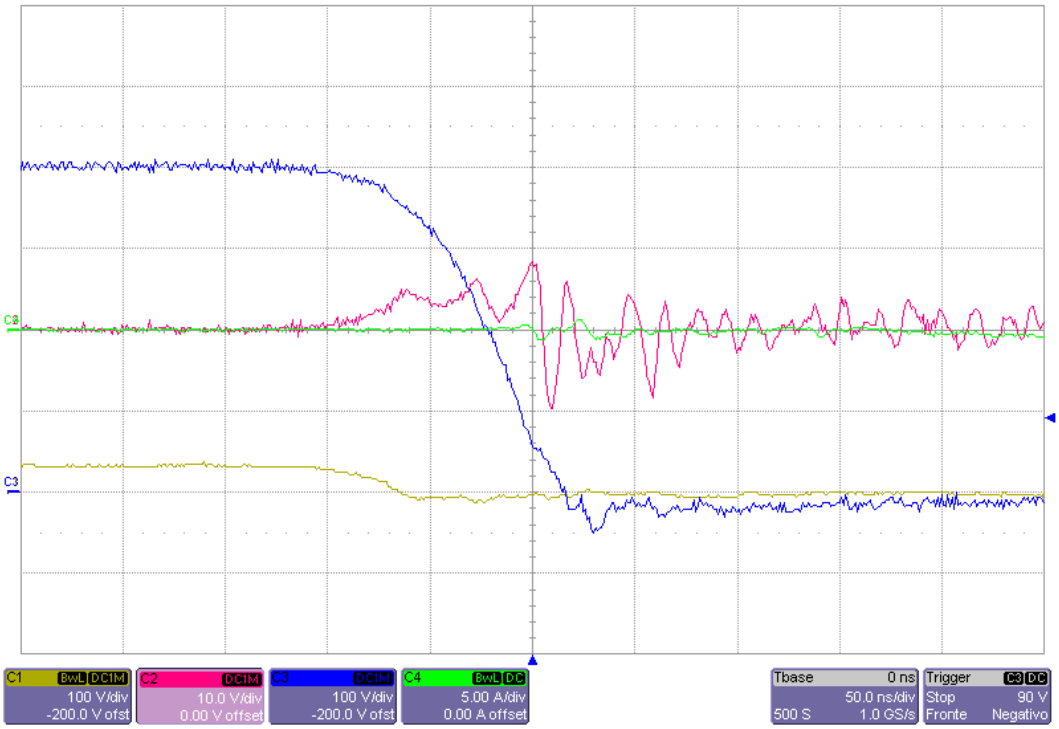


Figure Nº 63: Turn-OFF commutation (Time scale: 50ns/div)

Red Line: PASR voltage (10V/div)

Blue Line: Turn-ON commutation right leg (100V/div)

Green Line: PACR primary coil current (Inverted) (5A/div)

Yellow line: PACR primary coil voltage (100V/div)

From the beginning of commutation voltage transition is controlled, into very start leg capacitance is large so $^{dv}/_{dt}$ is controlled, when output capacitance decrease abruptly is necessary to use the snubber, this is verified because voltage transition slope is totally controlled. Then into final phase of transition clamped capacitor act reducing the overvoltage to less than 40V and also damping the waveform, turning back to zero volts with almost a first order dynamic. Is possible to support, turn-OFF commutation is Fully Compatible and Overvoltage less.

4.2.2 Quantitative Analysis

Experimental results were obtained by measuring losses, in the followings measures and calculations are reported according to Chapter III.

Is important to note that VSIL with IHC structure presents many freedom degrees and consequently find a global optimal will depend on many variables, first reported results were obtained with certain variables and is the 1st local optimal obtained, then a second group of results is reported where a 2nd optimal was found achieving best performance.

4.2.2.1 1st local optimal results:

Table N° 5: Experimental measures and calculations of losses for 1st local optimal

IL [A]	**20,01**	**18,01**	**16,01**	**15,01**	**14,02**	**12,01**	**10,00**	**8,03**
$V_{DC\text{-}LINK}$ [V]	400,00	400,00	400,00	400,00	400,00	400,00	400,00	400,00
$I_{DC\text{-}LINK}$ [mA]	87,86	75,61	62,83	58,19	53,40	45,38	39,46	23,49
$P_{DC\text{-}LINK}$ [W]	35,14	30,24	25,13	23,28	21,36	18,15	15,78	9,40
$V_{PACR\text{-}SX}$ [V]	63,30	64,70	66,10	67,00	67,70	69,00	70,40	68,50
$I_{PACR\text{-}SX}$ [mA]	139,09	115,87	94,43	84,81	75,53	58,06	43,06	67,84
$P_{PACR\text{-}SX}$ [W]	8,80	7,50	6,24	5,68	5,11	4,01	3,03	4,65
$V_{PACR\text{-}DX}$ [V]	61,30	61,20	61,20	61,10	61,10	61,10	61,10	61,30
$I_{PACR\text{-}DX}$ [mA]	127,81	107,51	88,70	79,90	71,32	53,67	35,63	62,33
$P_{PACR\text{-}DX}$ [W]	7,83	6,58	5,43	4,88	4,36	3,28	2,18	3,82
V_R [mV]	1316,00	1199,00	1065,00	993,00	925,00	792,00	670,00	570,00
$(R_{ON})_{LOOP}$ [mΩ]	80,98	82,45	82,48	82,06	81,93	81,80	82,70	87,46
P_{TOT} [W]	51,78	44,32	36,80	33,84	30,83	25,44	20,99	17,86
P_{COND} [W]	32,41	26,74	21,14	18,48	16,09	11,80	8,27	5,64
P_{COMM} [W]	18,17	16,38	14,46	14,16	13,54	12,44	11,52	11,02
$(P_{IHC})_{LL}$[W]	1,20	1,20	1,20	1,20	1,20	1,20	1,20	1,20
Comm Losses [%]	0,114	0,114	0,113	0,118	0,121	0,129	0,144	0,172

(*) All yellow cells are measured values.

(**) Voltage Supply V_{PACR} capacitive losses are calculated using 25pF, 400V, 30 kHz.

Right away useful graphs are reported in order to better understand and observe the effectiveness of the IHC structure:

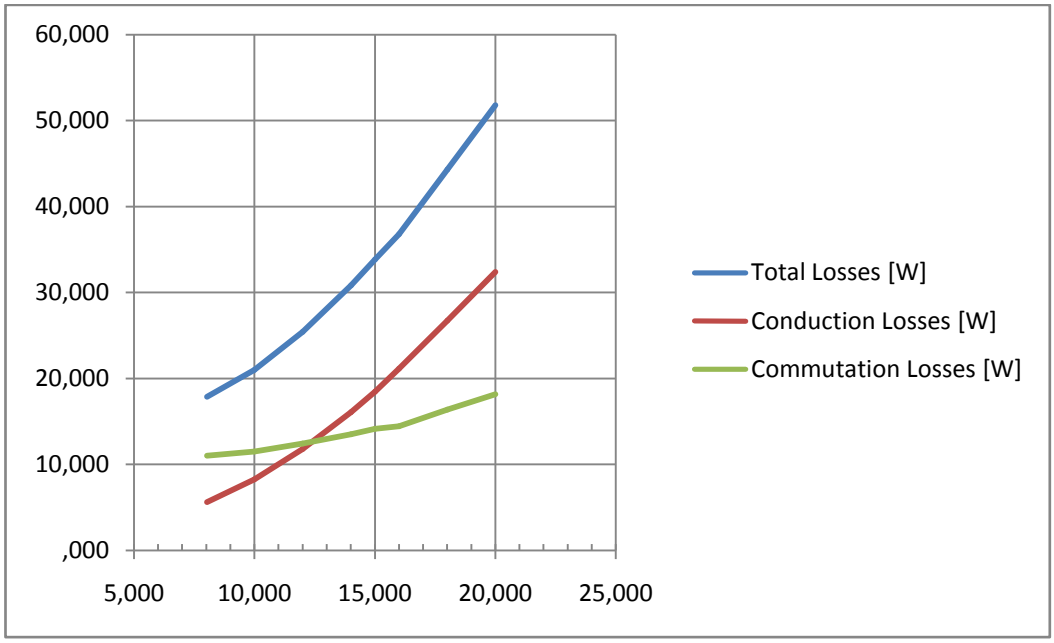


Figure Nº 64: Losses [W] vs. Switched current [A];

$$V_g = 400V, f_{sw} = 30\ kHz$$

Is possible to note that total and conduction losses have similar behaviour, when current increases conduction losses increases as well but commutation losses remains barely constant, this fact shows how commutation losses are limited.

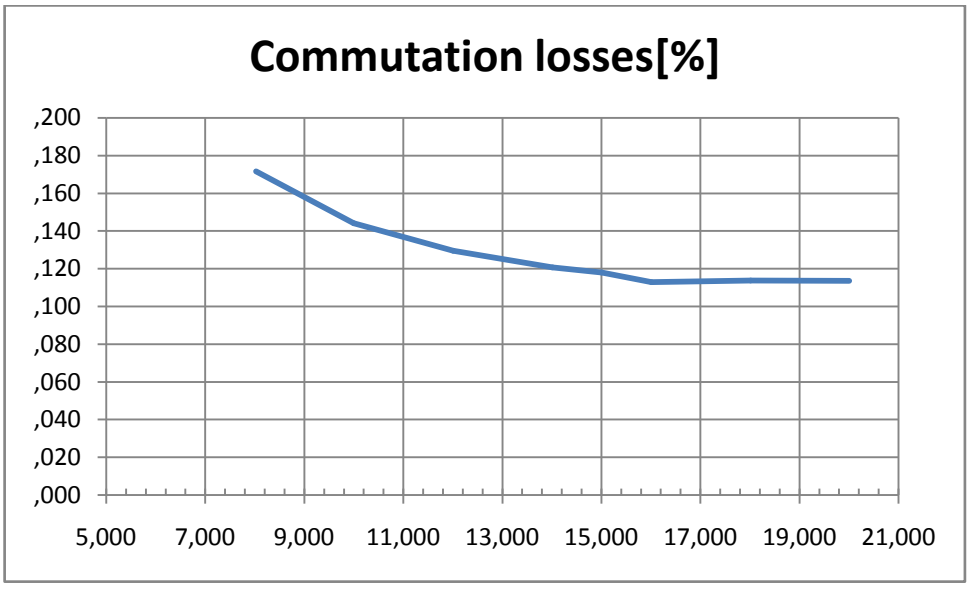


Figure Nº 65: 1st local Commutation Losses [W] vs. Switched current [A];

$$V_g = 400V, f_{sw} = 30\ kHz$$

As previously referred, an optimal point was found for the structure, experimental modifications were done and was possible to verify that some diodes reverse recovery affects importantly structure efficiency, the optimal solution is reported as follows:

4.2.2.2 2nd local optimal results:

Table Nº 6: Experimental measures and calculations of losses for 2nd local optimal

IL [A]	10,03	15,01	20,03	25,03
$V_{DC-LINK}$ [V]	400,85	400,20	400,05	400,15
$I_{DC-LINK}$ [mA]	35,70	53,11	79,36	114,50
$P_{DC-LINK}$ [W]	14,31	21,25	31,75	45,82
$V_{PACR-SX}$ [V]	75,00	75,00	75,40	71,60
$I_{PACR-SX}$ [mA]	40,50	72,85	111,90	161,50
P_{PACR}-SX [W]	3,04	5,46	8,44	11,56
$V_{PACR-DX}$ [V]	75,00	75,00	75,30	73,00
$I_{PACR-DX}$ [mA]	34,00	60,50	97,10	146,00
$P_{PACR-DX}$ [W]	2,55	4,54	7,31	10,66
V_R [mV]	630,000	917,00	1212,00	1481,00
$(R_{ON})_{LOOP}$[mΩ]	78,99	77,11	76,38	74,75
P_{TOT} [W]	19,90	31,26	47,50	68,04
P_{COND} [W]	7,94	17,36	30,63	46,83
P_{COMM} [W]	10,76	12,69	15,67	20,01
$(P_{IHC})_{LL}$[W]	1,20	1,20	1,20	1,20
Comm Losses [%]	0,134	0,106	0,098	0,100

(*) All yellow cells are measured values.

(**) Voltage Supply V_{PACR} capacitive losses are calculated using 25pF, 400V, 30 kHz.

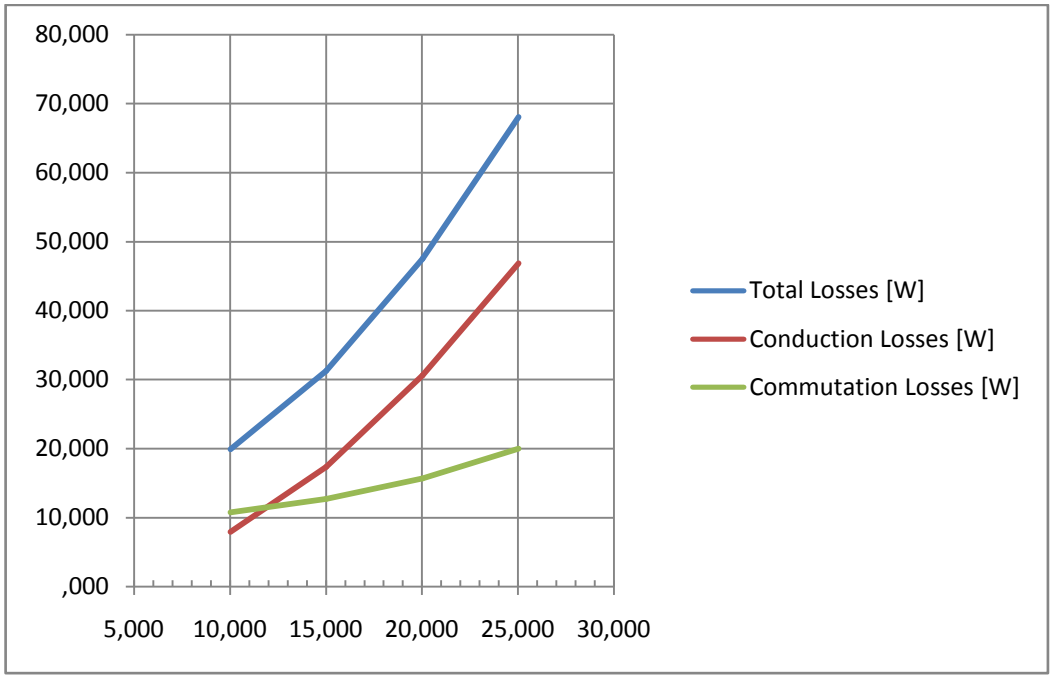


Figure Nº 66: Losses [W] vs. Switched current [A];

$$V_g = 400V, f_{sw} = 30\ kHz$$

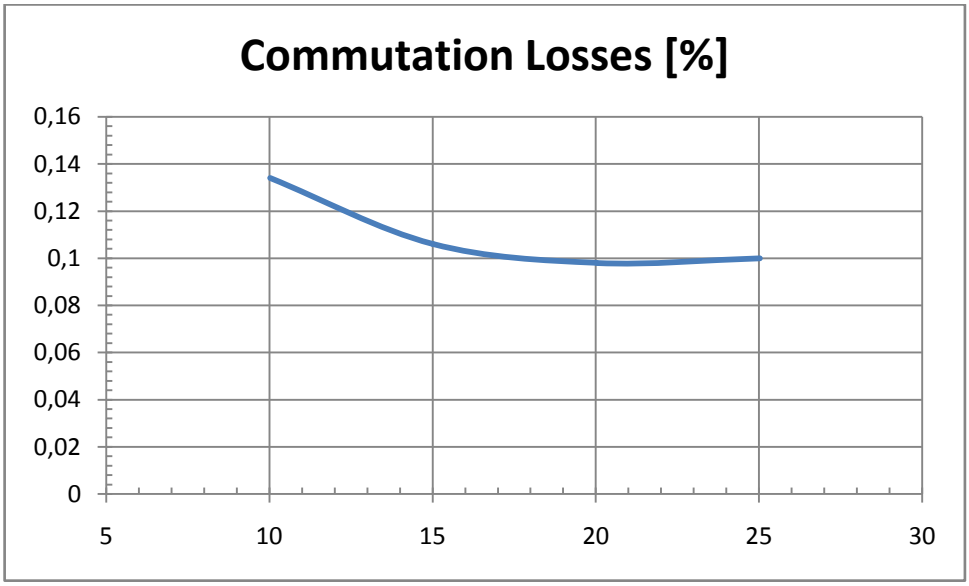


Figure Nº 67:2nd Local optimal Commutation Losses [W] vs. Switched current [A];

$$V_g = 400V, f_{sw} = 30\ kHz$$

With the optimal solution commutation losses by leg are minimized even lower than 0.1% for a 20A switched current, verifying that's possible realize 2-

mosfet inverter leg and not only, high efficiency is reached. Obviously total losses are dominated by conduction losses which are unavoidable.

4.2.2.3 Contrast with state of the art Power Module

In order to fix the ideas with a final contrast, an Infineon Power Module will be used to compare the commutation losses with the 2-mosfet VSIL even when a power module is a compact structure specially designed for power applications, while VSIL is realized with discrete components not designed for this kind of uses; datasheet information related with commutation losses are the followings:

Power Module: Infineon F4-30R06W1E3: $V_{CES} = 600V$, $I_{C_{nom}} = 30A$

Turn-ON energy loss per pulse: 75mJ @ $I_C = 30A, V_{CE} = 300V, V_{GE} = \pm 15V, T = 125°C$

Turn-OFF energy loss per pulse: 83mJ @ $I_C = 30A, V_{CE} = 300V, V_{GE} = \pm 15V, T = 125°C$

This represent a commutations equivalent time for leg $t_{eq} = 178\,ns$, which implies typical commutation losses: $P_{COMM} = 0{,}5\ \%$

In conclusion, specialized state of the art Power Modules (medium-power, low-voltage) actually available with similar nominal values are less efficient than 2-mosfets VSIL with IHC structure, and also being underutilized, switching only half of DC-link voltage.

CONCLUSIONS

Based on state of the art static conversion structures and components for low voltage and medium power is possible to understand that current technologies offers fasters switches (mosfets) with higher dynamics than currently used switches (IGBT) which means potential commutations losses reduction with nearby the same conductions losses, leading to an efficiency improvement.

A new structure is proposed for DC-AC conversion in order to exploit all the advantages that offers power mosfets and solving its strongly non linear behaviour by proposing an auxiliary system (as IHC) to allow ideal hard-switching commutation.

Experimental results show how ideal commutation waveform can be performed by dominating dynamic behaviour of the Voltage Supplied Inverter Leg becoming:

- Overcurrent less Turn-ON
- Quasi-Lossless Turn-ON
- Fully compatible commutations
- Overvoltage less commutations

Also is important to note that commutation efficiency improvement is outstanding reducing commutation losses to barely measurable levels.

The proposed inverter leg will be the next future of hard-switching not only for low voltage medium power applications but for high voltage and high power, taking into account technological advances that leads to fastest components but with barely null know-how to control this kind of components until now. Reducing the number of components from 4 to 2 on inverter legs will be not only a cost reduction but also an assembly simplification for high power applications considering big size components are used and simple fact of put together two power components instead of four represents a considerable benefit.

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