TRABAJO ESPECIAL DE GRADO

DISEÑO DE DEMOSTRADOR BACK-END PARA NUEVO SISTEMA RADAR DE NAVEGACIÓN

Presentado ante la Ilustre
Universidad Central de Venezuela
por el Br. Guerrero G., Gabriel G.
para optar al Título de
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(Laurea Specialistica in Ingegneria delle Telecomunicazioni)

Master Thesis

System Design of Novel Navigation Radar Demonstrator Back-End

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…To my parents Pedro Guerrero, Maria Guerra and Zoraida Guerra

in love and gratitude

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Guerrero G., Gabriel G.

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Palabras Claves: Sistema Radar; Radar de Navegación; Comercial off-the-shelf (COTS); Power Level Plan; Back-End; RASKEL; Secuencias Binarias; Algoritmo de búsqueda exhaustiva; Algoritmo evolutivo; Autocorrelación; Cross-correlación.

Resumen: El presente trabajo consiste en el diseño y construcción del primer demonstrador back-end para el nuevo sistema radar que está siendo actualmente desarrollado por el instituto Fraunhofer FHR. Este nuevo radar coherente de bajo costo para aplicaciones de navegación marítima, que usa arreglos de antenas activos de barrido electrónico (AESA) busca mejorar el desempeño que presentan los radares de navegación convencionales utilizando técnicas de integración de pulsos y de compresión de pulsos. Este trabajo inicia con una definición general de los sistemas radar y una introducción global del nuevo sistema radar en desarrollo mostrando sus principales características y los parámetros que deben ser considerados en el diseño del demostrador back-end. Consecutivamente el diseño final del back-end es presentado a el cual es aplicado el plan de nivel de potencia (power level plan). Este análisis permite estimar el nivel de potencia de señal y de ruido a lo largo de las cadenas de transmisión y de recepción. A continuación y para empezar el proceso de fabricación del demostrador se llevó a cabo selección de todos los componentes electrónicos commercial off-the-shelf (COTS) requeridos en el diseño. La técnica de compresión de impulsos usada implica la transmisión de secuencias de fase binarias. A fin de reducir las interferencias involucradas debido al uso de estas secuencias, un análisis detallado de los lóbulos laterales de la función de autocorrelación se llevó a cabo. Por lo tanto se indican los algoritmos matemáticos de búsqueda de códigos desarrollados y los resultados obtenidos con estos. Una nueva selección en función del máximo nivel de cross-correlación fue necesaria para minimizar la interferencia debida a los objetos situados fuera del rango de detección inequívoca del radar. Finalmente se muestran los resultados de las mediciones realizadas con el demostrador back-end construido con los dispositivos electrónicos previamente seleccionados.

SUMMARY

The first radar system was created in 1904 by the German Christian Hülsmeyer, who was the first to use radio waves to detect the presence of distant metallic objects but not its distance. His invention was developed for commercial application as it was used to detect approaching ships on the river. However, either the naval authorities or industry showed interest at that time. It was not until war world II when practical radar were secretly developed to meet the needs of the military applications, and until today this continues to be one of their main applications.

Due to the introduction of new low-cost and high performance radar systems, the design and manufacturing of commercial civilian radar system for a wide range of purposes have become exceptionally relevant, especially ship-borne and coast surveillance applications. In this field radar systems are widely used for target detection and collision avoidance. Conventional ship-borne navigation radar systems employ mechanically rotated antennas and non-coherent signals with high peak power usually generated by a magnetron. These characteristics require a constant maintenance and limit the general performance of the radar, without mentioning high operational costs. Currently, the department of antenna technology and electromagnetic modeling (AEM), of the Fraunhofer institute for high frequency physics and radar techniques (FHR) is working on the design and manufacturing of a novel low-cost coherent radar for maritime navigation with active electronically scanned array (AESA) antenna.

This new system uses coherent RF pulses enabling pulse integration and pulse compression techniques allowing to cover the same distance ranges with a lower peak signal power levels. Thus, there is no need for the magnetron. This system, in order to provide a large distance range of coverage, defines different operational modes, each covering a different radial range and using different pulse shapes. The structure of the radar is based on four active antenna front-ends arranged in a rectangular configuration, each with $\pm 45°$ coverage. The antenna front-end is basically composed by the RF feeding network, a large number of T/R modules and a linear array antenna of 109 identical monopoles inserted into a parallel-plate waveguide (PPW)

and a horn shaped section. Due to the modularity of the proposed system, also single front-ends may be used separately at critical position on a shore for coast or harbor surveillance.

This new radar system is expected to achieve all tasks of the conventional ship-borne navigation and coast surveillance radar system reducing as much as possible the manufacturing costs. The low manufacturing costs and also the innovation of this system is accomplished by using, in the system front-end, custom-made mixed-signal integrated circuits, mixed-signal printed circuit boards (PCBs) and a serial feeding network. The system back-end, on the other hand, reduces costs by utilizing low-cost commercial-of-the-shelf (COTS) components which are commonly used for wireless communication systems and wireless LAN. The system back-end refers to the part of the radar system where the amplification, shaping, modulation and filtering processes are implemented, not only for transmission but also for reception mode.

The objectives of this thesis involve the design and manufacturing of the first demonstrator of this new system back-end. The design process included a complete analysis of the signal and noise power levels along the transmitter and the receiver. On the other hand, the selection of all the suitable components, keeping always in mind to reduce as much as possible the manufacturing costs, was made as part of the manufacturing process.

The system back-end is the RF unit that is constituted by the transmitter and the receiver. The processes of amplification, shaping, modulation and filtering that accustom or refine the signal are performed in this unit. The transmitter must deliver a signal with the correct power level and shape to be transmitted depending on the selected operational mode. Therefore, the modulation of the signal to generate the pulses and sub-pulses necessary for the pulse integration and pulse compression techniques is made by this subsystem. The receiver, on the other hand, must amplify and refine the received low signal power level from the targets to detect and provide a suitable signal-to-noise ratio so the signal processing process that follows will be able to detect the target and determine correctly the distance at which it is placed. The design process of the system back-end was developed to satisfy the power requirements of the system front-end and the signal processing stage.

For the construction of the system back-end demonstrator an important design tool known as the power level plan was used. This analysis allows to determine the signal and noise power level along the transmitter and receiver chains due to a specific generated or received signal power level, respectively. In order to make the power level plan analysis as practical as possible, a constant update of the components' parameters was necessary, substituting the estimated values for those given by the selected component datasheets. The final power level plan was done using the measured values for the actual electrical specification of the selected components. This analysis improved the design process as it allowed to adapt the system back-end theoretical design to the commercial available components.

The pulse compression technique chosen to be used by this system implicated the generation of binary phased sequences. In order to reduce the interferences involved, a detailed analysis of the autocorrelation sidelobe level was performed, selecting for this system the sequences that provided the lowest sidelobe levels possible. The computational time required by a certain algorithm to calculate the maximum autocorrelation sidelobe level of all the codes of a certain length and select those who presented the smallest one, depends directly on their length. Due to the different sequence lengths required by the system's operational modes, the search for the most suitable codes could not be done with a single algorithm. In this thesis is presented an exhaustive search algorithm which provides as a result all the optimum sequences (minimum autocorrelation side lobe level) of a specific length. This algorithm is restricted by the practical computational time it should use, which for practical values permits results until a sequence length of about 40. Also in this work is presented the development of an evolutionary algorithm which allows to find near optimum codes within an acceptable computational time for sequence lengths up to 100 binary digits.

To avoid interference due to the objects placed outside the unambiguous range of the operational mode in used, different sequences must be used from one pulse to the next one based on the maximum cross-correlation level. For the sequences obtained by the developed algorithm a subsequent selection based on the maximum cross-correlation level was done.

The built demonstrator shown in this thesis, satisfied all power requirements and met the expected behavior predicted during the design

process and the power level plan analysis. However, future work and improvements must be done for this radar system back-end.

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LIST OF ACRONYMS AND ABBREVIATIONS

	Meaning
A/D	**A**nalog-to-**D**igital
ADC	**A**nalog-to-**D**igital **C**onverter
ADS	**A**dvance **D**esign **S**ystem
AEM	**A**ntenna Technology and **E**lectromagnetic **M**odeling
AESA	**A**ctive **E**lectronically **S**canned **A**rray
BiCMOS, BiMOS	**Bi**polar and **M**etal-**O**xide-**S**emiconductor
BPF	**B**and **P**ass **F**ilter
BPSK	**B**inary **P**ulse **S**hift **K**eying
COTS	**C**ommercial **O**ff-**T**he-**S**hell
CW	**C**ontinuous **W**ave
DPBA	**D**ouble **B**alanced **P**ower **A**mplifier
DUT	**D**evice **U**nder **T**est
EA	**E**volutionary **A**lgorithm
ENOB	**E**ffective **N**umber **o**f **B**its
ENR	**E**xcess **N**oise **R**atio
FFT	**F**ast **F**ourier **T**ransform
FHR	**H**igh **F**requency Physics and **R**adar Techniques
FPGA	**F**ield **P**rogrammable **G**ate **A**rray
GaAs	**G**allium **A**rsenide
HIS	**H**igh **I**solation **S**witch
IC	**I**ntegrated **C**ircuit
IFFT	**I**nverse **F**ast **F**ourier **T**ransform
IMD	**I**nter**M**odulation **D**istortion
IP_3/TOI	**T**hird-**O**rder **I**ntercept **P**oint
IQD	**I**&**Q** **D**emodulator
IVDS	**I**terated **V**ariable **D**epth **S**earch
LPF	**L**ow **P**ass **F**ilter
LNA	**L**ow **N**oise **A**mplifier

MF	**M**atched **F**ilter
NF	**N**oise **F**igure
PA	**P**ower **A**mplifier
PC	**P**ulse **C**ompression
PI	**P**ulse **I**ntegration
PRF	**P**ulse **R**epetition **F**requency
PS	**P**hase **S**hifter
PSL	**P**eak-**S**idelobe **L**evel
PSR	**P**eak-**S**idelobe **R**atio
p-p	**P**eak-to-**P**eak
RADAR	**Ra**dio **D**etection **a**nd **R**anging
RCS	**R**adar **C**ross **S**ection
RF	**R**adio **F**requency
RFIC	**R**adio **F**requency **I**ntegrated **C**ircuit
Rx	**R**eceiver
SiGe	**S**ilicon **G**ermanium
SNR	**S**ignal-to-**N**oise **R**atio
Tx	**T**ransmitter
TRM	**T**ransmitter-**R**eceiver **M**odule
TRM-IC	**T**ransmitter-**R**eceiver **M**odule **I**ntegrated **C**ircuit
VSWR	**V**oltage **S**tanding **W**ave **R**atio

Chapter 1

Introduction

1.1 Background and Motivation

Conventional ship-borne navigation and coast surveillance radar systems operating both in X-band or in S-band usually work with mechanically rotated antennas, and employ non-coherent signals with high peak power. The RF high power pulses are generated typically by a magnetron which together with the rotating antenna require frequent maintenance, produce high operational costs and limit the general performance of the conventional radar systems. These characteristics make the target detection and tracking a task considerably difficult to achieve.

The German company SAM Electronics GmbH (hereinafter referred to as SAM) which is one of the major suppliers for sophisticated Shipboard Degaussing Systems of various configurations for all types of naval vessels, initiated a study to establish if would be possible to build an S-band maritime radar system that eliminates the magnetron and employs electronically controlled array antennas. This new system design must meet all international performance requirements. This means, among other things, that the radiated power can be lower than the one of systems currently marketed, but the range must remain the same. As a further constraint, the production costs must be as low as possible. At the beginning it was desirable that the production costs were below 1.5 times the costs of the current

system. If it is possible to establish such a system, the company SAM wanted to know who could develop this system.

Against this backdrop the Research Society of Natural Sciences FGAN through its Research Institute for High Frequency Physics and Radar Techniques (FGAN-FHR) in Wachtberg, Germany decided to follow through, in 2007, the study and development of this new system which has been baptized as RASKEL (study feasibility of a S-band radar for maritime navigation with coherent signal processing and/or electronically controlled antenna). This project was funded by SAM just during its first year. The development of the demonstrator has been, since then, carried out and funded by FGAN-FHR alone. Meanwhile FGAN-FHR has become an institute of the Fraunhofer Society for the advancement of applied research (German: *Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung e. V.*) changing its name to Fraunhofer FHR.

Currently, the department of antenna technology and electromagnetic modeling (AEM) of the Fraunhofer FHR has initiated the development of a low-cost coherent radar system demonstrator employing active electronically scanned array (AESA) antennas for maritime applications. The RF system uses coherent RF pulses enabling pulse integration and pulse compression techniques. Defining different operational modes, each covering a different radial range region and employing different pulse shapes. Four active antenna front-ends are arranged in a rectangular configuration in order to ensure 360° coverage. Each one of these consists of a linear array antenna composed by one hundred nine (109) Transmit/Receive-modules, and a series feeding network.

This project have been motivated by the fact that since 2007 the international performance requirements and methods of testing for commercial maritime navigation radar systems [Int07] dispose of the stringent usage of short RF transmit pulses with high peak power for S-Band systems, adding consequently to the design of a future S-band ship radar system a number of new degrees of freedom. The radar systems now could operate with lower transmit power and maintain their coverage or even improve it through the use of coherent signals. To generate a lower transmission power a magnetron is not needed anymore and other antenna types can be also employed. The proposed system is expected to cover all tasks of the

conventional ship-borne navigation and coast surveillance radar system. The RF system will be also able to perform many other new tasks because of the agility of the AESA antennas and the prospects of coherent signal processing. Additionally it should be possible, due to such an improved on S-Band Radars, to reduce the cost so the total system costs maintains below 1.5 times the cost of conventional radars. However, last estimations shown that the manufacturing of this new system will require a higher price.

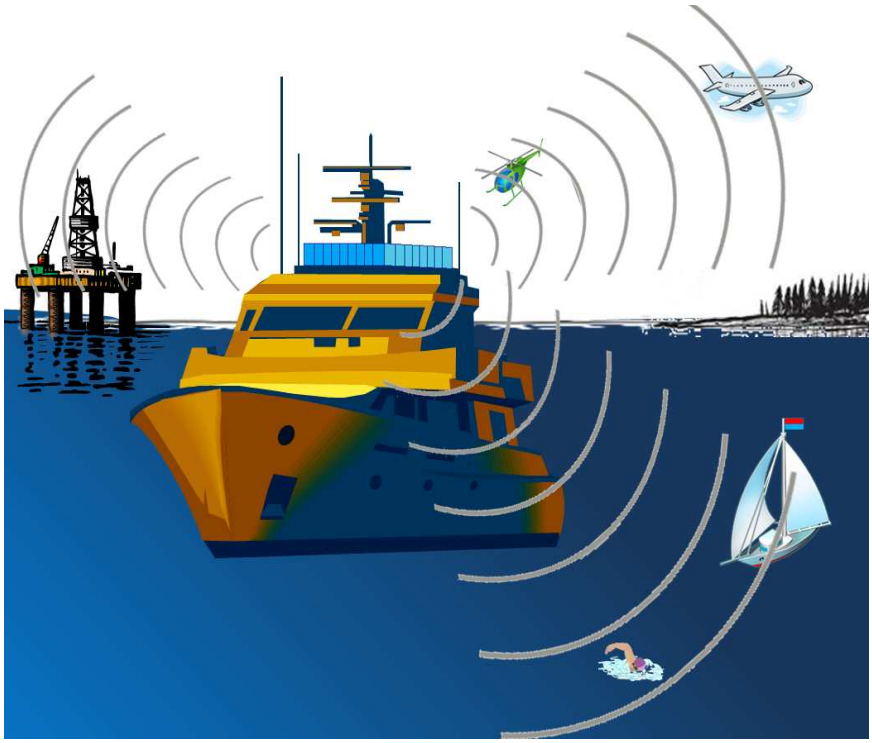


Figure 1.1.1: Potential new applications of the proposed system in addition to conventional navigation support.

This system, for an easier analysis and development, has been divided in three main sub-systems know as front-end, back-end and signal processing stage. The front-end sub-system is responsible for collecting all the different input signals and to process them in a way to match with the back-end input specifications. This sub-system is basically composed by the RF feeding network, a large number of T/R modules and a linear array antenna of 109 identical monopoles inserted into a parallel-plate waveguide (PPW) and a

horn shaped section [BPK10a]. The system back-end refers to the stage where the amplification, shaping, modulation and filtering processes are implemented, not only for transmission but also for reception mode. This sub-system is constituted by the electronic devices that compose the transmission and reception path. At last the signal processing is a software based stage which extracts the target information from the echo signals already refined by the back-end [BPK10b].

In this document an overview of the novel navigation radar demonstrator will be given. Emphasis will be placed on the design, feasibility and selection of commercial low-cost components, and construction of the first prototype of the radar system back-end.

1.2 Problems and Objectives

SAM was interested in knowing if and how it is possible to produce an S-band radar system that eliminates the necessity of the magnetron for the generation of the radar signal pulses and that substitutes the mechanical rotating antenna by an electronically controlled antenna. This system must meet the applicable standards from July 2008, where it is established that preserving the same operational range, the radiated power can be lower than the one used by the conventional radar systems. This system also must have the production cost as low as possible. Fraunhofer FHR is in charge of the development of this project which has been divided in two sub-projects so far: the design of the system front-end and design of the system back-end.

In respect of the system back-end design, which is the main purpose of this thesis, it must meet the power requirements of the system front-end in order to achieve the transmission of the radar pulses successfully. Simultaneously, it must meet power and noise requirement of the signal processing unit to assure the correct interpretation of the echo signals received by the system front-end. As a further constraint and in order to conform to the reduction of the production costs of the entire radar system, the system back-end must reduce its production costs as much as possible by basing its design on COTS (commercial-off-the-shell) components.

The objectives of this thesis are:

- Design of the transmitter and receiver path that compose the system back-end considering all the signal and noise power requirements given by [Ber07a] and Fraunhofer FHR.
- Due to the three operating modes established during the radar system design, the transmitter must be capable of generating the different pulse shapes required.
- Search and selection of the COTS components that satisfy the requirements in order to reduce as much as possible the production costs. In case no suitable COTS components can be found, the design of the missing components must be done. The components available at or manufactured by Fraunhofer FHR have to be considered.
- Development of an algorithm that allows to find the binary phased sequences necessary for the pulse compression technique, with the lowest maximum autocorrelation sidelobe level in order to reduce possible interferences at the signal processing stage due to the high autocorrelation sidelobe levels.
- Construction of the first system back-end demonstrator with the selected components where the requirements of gain and noise figure are satisfied for both transmission and reception mode.

1.3 Outline of the Thesis

The basic principles of operation regarding radar systems and a formal description of the RASKEL project and the radar system under development follow this introductory chapter. The fundamentals of the system front-end are also introduced in Chapter 2 but as its design is not covered by this thesis it is recommended to consult [Ber07a] and [Erk09] for a deeper understanding of the radar system. This chapter also includes the system parameters that had to be considered for the system back-end design. The full explanation of the system back-end design and the innovation factor attached to it are presented in Chapter 3. The power level plan where the gain requirements of

the reception and transmission path are estimated is described in Chapter 4. In this chapter the signal and noise power level at all the stages of the transmitter and receiver are illustrated. Chapter 5 introduces all the different COTS components that were selected for the construction of the system back-end demonstrator, listing also their main features. An overview of the algorithms designed to find the suitable binary pulse compression codes that will be used by the radar system is separately documented in Chapter 6. The full description of the measurement procedures that were executed on all the selected components and the results of the measurements that were made on the first system back-end demonstrator are concentrated in Chapter 7. Finally, Chapter 8 summarizes and concludes the thesis and gives an outlook on the improvements that have been not implemented yet.

Chapter 2

Radar System Basic and Design

2.1 Basic Radar System Architecture and Operation

The term Radar is the acronym derived of "Radio Detection and Ranging". It refers to the electronic equipment that detects the presence, direction, height, speed and distance of objects by using reflected electromagnetic energy [Sko81]. Radar is unaffected by darkness and also penetrates weather. This permits radar systems to determine the position of ships, planes, cars, spacecraft, people and even land masses that are invisible to the naked eye because of distance, darkness, or weather. The radar antenna transmits pulses of radio waves or microwaves which bounce off any object in their path. The object returns a tiny part of the wave's energy to an antenna which is usually located at the same site as the transmitter. The radar then reads this returning signal and analyzes it.

Radar units are usually design to work with very high frequency due the high resolution (the radar is able to detect smaller objects) that these frequencies allow. Another reason for the use of high frequencies is that the higher the frequency, the smaller the antenna size at the same gain.

The operation of a typical pulse radar may be described with the help of the block diagram shown in Fig. 2.1.1. This block diagram is a simplified version that omits many details and it does not include several devices often found in radar.

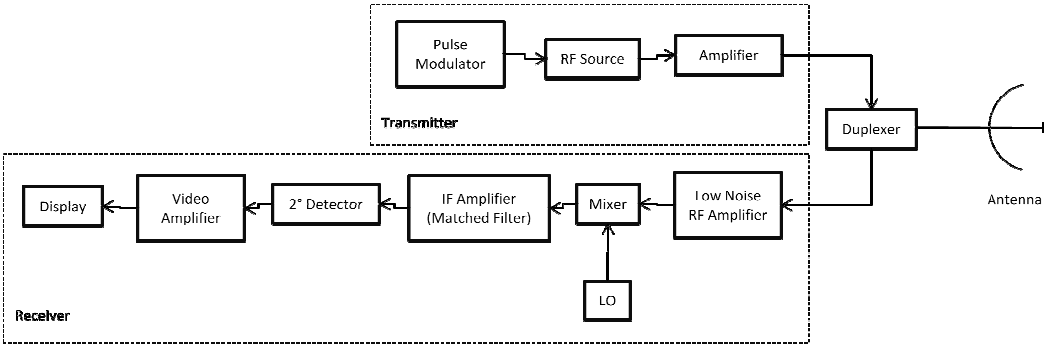


Figure 2.1.1: Block diagram of a pulse radar from [Sko81].

For traditional radar systems the high electromagnetic power that must be delivered by the RF source may be obtained with the use of a magnetron that is turned on and off as the Pulse Modulator commands in order to generate a repetitive train of high power pulses. For the construction of the radar transceiver a single antenna is most likely used, that is why a duplexer has got to be implemented. The simplest duplexer that could be used is a ferrite circulator which can provide the receiver with an echo signal during the transmission time, having no limitations of blind distance. Unfortunately, it is complicated to build circulators that can perform up to many 100 kW in the practice, leaving the circulators as predetermined duplexers for radar system with a very low transmitter's power.

An electronic switch can also be used as a duplexer, this must alternately switch the antenna between the transmitter and receiver mode. Unfortunately, it needs a recovery time situated in the nanosecond range. This time represents the delay between end of transmission and beginning of echo reception, and it determines the minimum distance from the radar antenna towards the nearest object that can be detected [Erk09].

The receiver is usually of the super-heterodyne type. The first stage as shown in Figure 2.1.1 is a low noise RF amplifier which is placed after the antenna to reduce losses in the feed line, and also because the effect of the noise from subsequent stages of the reception path will be reduced by its gain. The mixer and the local oscillator convert the RF signal to an intermediate frequency IF. In order to maximize the signal-to-noise power ratio at the output, the IF amplifier should be designed as a matched filter. Then, the pulse modulation is extracted by the second detector and amplified by the

video amplifier to a level where it can be properly displayed, usually for a cathode-ray tube (CRT).

The directivity of the radar antenna establishes the angular determination of the target. The antenna directivity D_A defines the ability of the antenna to concentrate the energy transmitted in one particular direction. The elevation and azimuthal angle from the radar antenna to the target can be found by measuring the direction in which the antenna is pointing when the echo signal is received. The directivity is function of the size of the antenna and the wavelength.

The angle between the true north and the straight line pointed directly to the target represents the true bearing. This angle is measured in the horizontal plane and in a clockwise direction from the north. For most of the radar systems the antennas have been designed to radiate energy in one main beam that can be moved in bearing by simply moving the antenna. In practice, search radar antennas move continuously and the point of maximum echo is when the beam points directly to the target [Sko81].

As has been implied before, the most common radar waveform is a train of narrow, rectangular-shaped pulses modulating a sine wave carrier. These pulses are repeated with a certain *pulse repetition frequency* (PRF). The distance or range from the radar system to the target is determined by measuring the time t_d taken for one transmitted pulse to travel to the target and back. Since electromagnetic energy propagates at the speed of light, the range R is:

$$R = \frac{c \cdot t_d}{2} \tag{2.1.1}$$

where $c \approx 300\ Km/s$.

Once the first pulse is transmitted, a sufficient length of time must pass to allow any echo signals to return and be detected before the next pulse may be transmitted. Therefore the pulse repetition frequency is fixed based on the largest distance at which targets are expected. With this consideration it is possible to determine the range beyond which targets appear as "second-time around", which means that the echo signals coming from these targets might arrive after the transmission of the next pulse causing ambiguities in

the measuring range. This range is called the maximum unambiguous range and is:

$$R_{unamb} = \frac{c}{2 \cdot PRF} \tag{2.1.2}$$

Even if the typical radar system uses pulse-modulated waveforms, there are other suitable modulations that might be used. For example, continuous waveform (CW) could be used in order to take advantage of the Doppler Effect to separate the received echoes from the transmitted signal, and the echoes from the stationary clutter [Sko81].

The minimum detectable range (or blind distance) is also important. When the leading edge of the echo pulse falls inside the transmitted pulse, it is impossible to determine the "round trip time", which means that the distance cannot be measured. The minimum detectable range R_{min} depends on the transmitted pulse with $\boldsymbol{\tau}$, and the recovery time $t_{recovery}$ of the duplexer as is shown by Eq. (2.1.3). The receiver does not listen during pulse transmission, because it needs to be disconnected from the transmitter during transmission to avoid damage. In that case, the echo pulse comes from a very close target. Targets at a range equivalent to the pulse width from the radar are not detected.

$$R_{Blind} = \frac{c \cdot (\tau + t_{recovery})}{2} \tag{2.1.3}$$

2.2 Radar Equation

The characteristics of the transmitter, receiver, antenna, target, and environment can be related to the range of the radar by means of the radar equation. The use of this equation is not only to assist in the design of radar systems to meet the detection specifications set by the users but also provides a means for predicting signal-to-noise ratios, and for predicting the maximum range at which targets with given radar cross section (RCS) will produce a specified signal-to-noise ratio (SNR).

If the power of the radar transmitter is denoted by P_t, and if an isotropic antenna is used (one which radiates uniformly in all directions), the power density at the distance R from the radar is equal to the transmitter power divided by the surface area $4\pi R^2$. As practical radar systems employ directive antennas to channel the radiated power into some particular direction, this expression is affected for the measure of the increased power radiated in the direction of the target as compared with the power that would have been radiated from an isotropic antenna. This measure is known as the antenna gain G_A. The power density at the target from an antenna with a transmitting gain G_A is:

$$S_t = \frac{P_t \cdot G_A}{4\pi R^2} \tag{2.2.1}$$

The target detection depends not only on the power density at the target position but on how much power is reflected by the target in the direction of the radar as well. The size and ability of a target to reflect radar energy can be summarized into a single term, σ, known as the radar cross section, which is a measure of the target size as seen by the radar. Therefore the power density at the radar due to the reflection from the target is:

$$S_r = \frac{P_t \cdot G_A}{4\pi R^2} \cdot \frac{\sigma}{4\pi R^2} \tag{2.2.2}$$

The portion of the echo power that is intercepted by the radar antenna is determined by its effective area A_e. As a result, the power P_r received by the radar corresponds to:

$$P_r = \frac{P_t \cdot G_A \cdot \sigma \cdot A_e}{(4\pi)^2 \cdot R^4} \tag{2.2.3}$$

Antenna theory gives the relationship between the transmitting gain and the receiving effective area as:

$$G_A = \frac{4\pi \cdot A_e}{\lambda^2} \tag{2.2.4}$$

Consequently the antenna provides the received power

$$P_r = \frac{P_t \cdot {G_A}^2 \cdot \sigma \cdot \lambda^2}{(4\pi)^3 \cdot R^4 \cdot L} \tag{2.2.5}$$

The parameter L represents the losses between transmitter output and receiver input thus modeling all losses caused by switches, antenna, atmosphere, etc.

The maximum radar range R_{max} is the distance beyond which the target cannot be detected. It occurs when the received echo signal power P_r just equals the minimum detectable signal S_{min}. Therefore

$$R_{max} = \sqrt[4]{\frac{P_t \cdot {G_A}^2 \cdot \sigma \cdot \lambda^2}{(4\pi)^3 \cdot S_{min} \cdot L}} \tag{2.2.6}$$

Eq. (2.2.6) is the simplest representation of the radar equation.

2.3 Receiver Noise

The sensitivity of a radar receiver is determined by the unavoidable noise that appears at its inputs. At microwave radar frequencies, the noise that limits the detection is usually generated by the receiver itself rather than by external noise that enters the receiver via the antenna. In the ideal case where the radar operates in a perfectly noise-free environment, and the receiver itself were so perfect that it does not generate excess noise, there still will be present the thermal noise which is the noise component generated by the thermal motion of the conduction electrons in the ohmic portions of the receiver input stages.

The noise in a receiving system can be also from other noise-generating processes, which most of them generate noise whose spectrum and probability distributions are similar to thermal noise [Sko81]. For this reason all noise sources can be gathered together and considered as thermal noise. The thermal noise power is characterized as follow

$$N_o = k \cdot T_o \cdot B_w \tag{2.3.1a}$$

where: $k = 1.38\,x\,10^{-23}\ \frac{J}{K}$ (Boltzmann's constant).

B_w represents the noise bandwidth.

T_o is the system noise temperature which is equal to the IEEE standard temperature $(290\,K)$.

The noise quantity $k \cdot T_o \cdot B_w$ is known as the minimum output noise power or "Thermal Noise" N_o, only reachable by an ideal receiver. Noise at the output of a practical receiver is always greater by a factor F expressed in Decibels and known as the noise figure. So the equation (2.3.1a) can be rewritten as

$$N = k \cdot T_o \cdot F \cdot B_w \tag{2.3.1b}$$

The noise figure is a measure of the degradation of the signal-to-noise ratio, caused by components in the RF signal path, for a specific bandwidth. The noise figure of a receiver or any single electronic component, in case of pure thermal noise at its input, can be expressed as:

$$F = \frac{\left(\frac{S_i}{N_i}\right)}{\left(\frac{S_o}{N_o}\right)} \tag{2.3.2}$$

where: S_i and N_i are the signal and noise power at its input, respectively.

S_o and N_o are the signal and noise power at its output, respectively.

Considering now as an input signal S_{in} the minimum detectable signal for a minimum signal-to-noise ratio necessary for target detection at the receiver output $SNR_{out,min}$.

$$S_{min} = k \cdot T_o \cdot F \cdot B_w \cdot SNR_{out,min} \tag{2.3.3}$$

And substituting this expression in the Eq. (2.2.6) it is possible to calculate the maximum range in which it is possible to achieve detection respecting the SNR requirements established for the receiver.

$$R_{max} = \sqrt[4]{\frac{P_t \cdot {G_A}^2 \cdot \sigma \cdot \lambda^2}{(4\pi)^3 \cdot k \cdot T_o \cdot F \cdot B_w \cdot SNR_{out,min} \cdot L}} \tag{2.3.4}$$

2.4 Pulse Integration

Coherent Pulse Integration is a signal processing technique that allows the enhancement of the SNR as a result of the inability to generate high energetic radar pulses that ensure a large echo signal for large maximum ranges, which is the major limitation of the conventional radar systems, particularly for semiconductor driven radar. The pulse integration employs the transmission of several pulses rather than a single pulse. The number of pulses transmitted and received corresponds with the notation N_p. Before the detection, the receiver takes a coherent sum over all the pulses (i.e. with the same phase). Random events like noise will not occur in every pulse and therefore, when averaged, will have a reduced effect as compared to actual targets that will be detected transmitting a single pulse.

The efficiency of coherent pulse integration can be determined as follows. The full procedure is shown in [Erk09]. Knowing that the received signal is composed by a signal and a noise component, with $r_m(t)$ defined as the m-th pulse received

$$r_m(t) = s(t) + n_m(t) \tag{2.4.1}$$

where $s(t)$ represents the signal content and $n_m(t)$ is the additive white Gaussian noise for the m-th pulse. As the objects to be detected are slow and the used pulses are short, the fluctuations for the signal during a pulse train are low, therefore $s(t)$ is approximately equal for $m = 1 \dots N_p$.

Assuming Pulse Integration is conducted ideally and lossless, the resulting signal coherent average becomes:

$$r_{average}(t) = \frac{1}{N_p} \cdot \sum_{m=1}^{N_p} r_m(t) = \sum_{m=1}^{N_p} \frac{1}{N_p} \cdot [s(t) + n_m(t)] \tag{2.4.2a}$$

$$r_{average}(t) = s(t) + \sum_{m=1}^{N_p} \frac{n_m(t)}{N_p} \tag{2.4.2b}$$

The noise power accumulated over all N_p pulses is equal to the variance

$$\psi_{np}^2 = E\left[\left(\sum_{m=1}^{N_p}\frac{n_m(t)}{N_p}\right)\cdot\left(\sum_{m=1}^{N_p}\frac{n_m(t)}{N_p}\right)^*\right] \tag{2.4.3}$$

where E equals the expected value operator. Thus

$$\psi_{np}^2 = \frac{1}{{N_p}^2}\cdot\sum_{m,k=1}^{N_p}E[n_m(t)\cdot n_k^*(t)] = \frac{1}{{N_p}^2}\cdot\sum_{m,k=1}^{N_p}\psi_{n1}^2\cdot\delta_{mk} = \frac{\psi_{n1}^2}{N_p} \tag{2.4.4}$$

where: δ_{mk} equals unity for $m = k$ and zero else.

ψ_{n1}^2 is the single pulse noise power.

In the average, the signal power remains the same as for a single pulse while the noise power is reduced by a factor N_p. As a result, the signal to noise ratio of coherent pulse integration radar is N_p times the SNR of a single pulse radar.

$$SNR_{PI} = N_p\cdot SNR_1 \tag{2.4.5}$$

From Eq. (2.3.4) the new radar equation with coherent pulse integration knowing that the maximum range operation is effectively expanded by the number of processed pulses, is equal to:

$$R_{max} = \sqrt[4]{\frac{P_t\cdot G_A\cdot A_e\cdot\sigma\cdot N_p}{(4\pi)^2\cdot k\cdot T_o\cdot F\cdot B_w\cdot L\cdot SNR_{out,min}}} \tag{2.4.6}$$

The maximum number of pulses that can be transmitted per antenna beam step is limited by the pulse repetition frequency PRF and by the fact that a 360° scan is required to be repeated regularly. The maximum number of pulses that can be transmitted per angle step equals:

$$N_p^{max} = \frac{\theta_a\cdot PRF}{\dot{\theta}_{scan}} \tag{2.4.7}$$

where $\dot{\theta}_{scan}$ represents the angle to be scanned in one second and θ_a is the angular precision.

Throughout this analysis have been neglected some non-idealities that reduce the efficiency of the coherent integration. The more significant effect is

the loss due to antenna rotation. As the beam position of a phased array is fixed and then moves on in a discrete time instant, the losses for a fraction of the pulses (i.e. the fraction of the scan time in which the object is illuminated with maximum gain as a result of the antenna moving from one beam position to the next one) are not existent. All the other possible additional losses have been considered in a loss overhead as part of system budget and is shown in table (2.7.3).

2.5 Pulse Compression

Pulse compression is a generic term that describes a wave shaping process that is used to compensate the limited peak power available for transmission. The reason behind the origin of the pulse compression is the desire to amplify the transmitted impulse power by temporal compression. As well as pulse integration, this technique has as an aim to raise the receiver SNR, increasing the average transmitted power [Erk09]. To do this at the transmitter is necessary to generate pulses with longer duration. The radar signal bandwidth relates to the pulse duration τ as:

$$B = \frac{1}{\tau} \tag{2.5.1}$$

Due the time extension, the bandwidth of the signal decreases. Since a low bandwidth B results in a low radial resolution ΔR, this effect is not desirable.

$$\Delta R = \frac{c_o}{2 \cdot B} \tag{2.5.2}$$

where c_o equals to the speed of light.

The Pulse compression combines the high energy of a longer pulse with the high resolution of a short-pulse width. The use of this technique means to modulate the radar pulse with some sort of phase or frequency modulation, in order to increase the bandwidth and, thus the radial range resolution. Noise bandwidth is enlarged at the same time and thus, the improvement in resolution needed for enhanced range accuracy is realized by correlating the

received signal with the modulation scheme which was used for pulses generation. To achieve this it is necessary the implementation of a match filter, where the output SNR at the time instant t_{max} for the correlation peak equals

$$\frac{SNR\ (t = t_{max})}{SNR_{MF_{in}}} = 2 \cdot B \cdot \tau \tag{2.5.3}$$

with $B \cdot \tau$ as the matched filter gain. At the end the SNR reduction is compensated by the matched filter. As a result the overall system SNR is untouched while the range resolution is enhanced at the cost of larger bandwidth occupation and increased requirement on the complete receiver circuitry.

The method that was chosen to be implemented in the proposed system was a BPSK (i.e. Binary Phase Shift Keying) modulation in order to generate phase-coded sequences. Here the long pulse that is going to be transmitted is sub-divided into a specific number of shorter sub-pulses of equal time duration; each is transmitted with a particular phase.

$$\tau_{sp} = \frac{1}{B_c} = \frac{\tau}{N_{sp}} \tag{2.5.4}$$

where: N_{sp} is the number of sub-pulses.

τ_{sp} is the sub-pulse duration.

B_c is the transmitted signal bandwidth.

The binary code then consist of a sequence of either +1 and -1, so the phase of the transmitted signal alternates between 0° and 180° in accordance with the sequence use as modulator signal.

Substituting Eq. (2.5.4) in Eq. (2.4.6), it is possible to observe how the use of pulse compression ideally adds new parameters to the radar equation.

$$R_{max} = \sqrt[4]{\frac{P_t \cdot G_A \cdot A_e \cdot \sigma \cdot N_p \cdot N_{sp}}{(4\pi)^2 \cdot k \cdot T_O \cdot B_c \cdot F \cdot L \cdot SNR_{out,min}}} \tag{2.5.5}$$

2.6 RASKEL System Overview

Before the characterization and design of the system back-end, here an overview of the entire radar system is presented providing in this way a general picture of the whole system. The new radar system (or RASKEL project as it has been baptize by Fraunhofer FHR) block diagram is shown in Figure 2.6.1, where the individual sub-systems are shown as boxes connected by control and signal paths. The front-end is the subsystem which determines the feasibility of the radar system significantly. It contains the actual innovations and the critical components. Deeper information about the design of the front-end system can be found in [Erk09] and [Ber07a]. The transmitter/receiver (back-end) is the subsystem on which this thesis is focused. The innovation of this subsystem is based on the use of low cost COTS (Commercial off-the-shell) components usually applied for wireless communication and wireless LAN. The remaining units of the whole system are described briefly below.

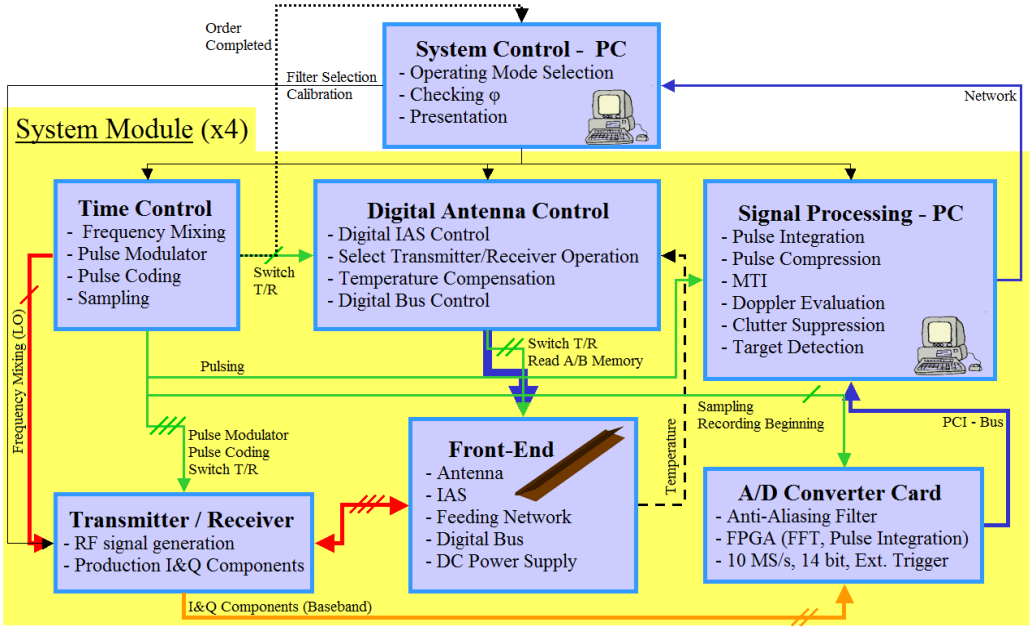


Figure 2.6.1: Block diagram of the entire radar system, sub-systems with control and signal paths [BPK10a].

As was previously introduced, for this new radar system the magnetron and the rotating antenna commonly utilized in a conventional system will be replaced by the implementation of coherent radar pulses and linear active electronically scanned array (AESA) antennas. The AESA is a type of phased array radar whose transmitter and receiver functions are composed of numerous small solid-state transmit/receive modules (TRMs). Each one of these small modules emits its own energy "beam", reducing in this way the electromagnetic emission and the probability to be detected.

As shown in the Figure 2.6.2, the total circumferential coverage is achieved by arranging four system modules in a rectangular configuration. Each system module, that includes an antenna front-end, and RF transmitter and receiver (back-end) and a signal processing unit, cover 90° in the azimuthal plane. These modules are controlled by a central unit that distributes observation tasks and displays the target positions.

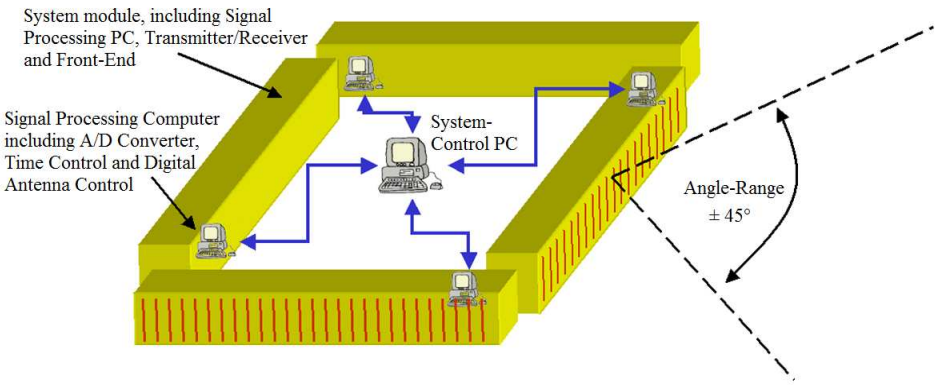


Figure 2.6.2: Schematic representation of the spatial arrangement of the system components [Ber07a].

Each one of the four system modules contains a local control unit realized by e.g. a personal computer (PC), which is responsible for the signal processing. Its purpose is to digitize the received signals and transmit them to the system-control PC. Depending on the operating mode not only pulse integration but pulse compression techniques can be performed as well. Portions of these computationally intensive tasks can already be realized by field programmable gate arrays (FPGAs) on the analog-to-digital converter (ADC) card plugged into a PCI slot of the PC. The ADC is equipped with

certain computational capabilities and can perform a fast Fourier transform (FFT) of the received signals before passing them to the signal processing unit. This card was implemented for the digitization of the Baseband I&Q components of received echo signals with a sampling rate equal to 10 MS/s and 14 bits resolution. In order to ensure synchronous sampling from pulse to pulse of the received signals, the sampling time must be controlled via an external trigger. In addition the trigger signal must be provide the timing where the ADC must start the recording of the received data.

On the one hand the transmitter/receiver block is responsible for the generation of the RF pulses to be transmitted, and must have sufficient power for further amplification by the active antenna. On the other hand, it adjusts the bandwidth and the power level of the received signal in such a way that this level matches the dynamic range of the A/D converter after down mixing the RF signal to baseband.

Since pulse integration and pulse compression techniques will be used, the critical relation between the transmit time and the sampling point is critical for this system. Therefore a dedicated time control for the transmitter/receiver must be available. The pulse coding to be performed in the designed system is a binary phased code. This process is known as Binary Phase Shift Keying (BPSK). The individual sub-pulses are transmitted with a specific phase delay of 0° or 180°. The binary phased sequences chosen to be used in the system are memorized and maintained to be available for each transmission time. The sequences are specified by the system control PC, and can also be changed from pulse to pulse in order to reduce the interference caused by other radar systems placed close enough and that could be working simultaneously to this system. Finally, the digital antenna control is responsible for switching the T/R modules between transmission and reception mode and setting all phase shifter states for the required scanning direction.

2.7 Novel Radar System Parameters

Based on the new performance standards for S and X-Band ship radar [Int07], performances standards and some additional guidelines were set by

SAM Electronics GmbH and Fraunhofer FHR. These parameters where chosen in order to achieve that performance of the novel low cost radar system to be at least equal to the performance of the conventional ones.

As this system has been designed to work in the S-Band, the frequency range corresponds to the part of the spectrum from 2.9 GHz to 3.1 GHz, typically using as the carrier frequency 3GHz.

The most important parameter to be determined in order to establish the technical feasibility of the coherent signal processing radar with electronically pointing antenna was the maximum transmit power of each AESA antenna's T/R-modules. As a core of these modules were developed integrated mixed-signal circuits in a 25nm SiGe BiCMOS technology with a maximum transit frequency of 75 MHz with the purpose of reducing the system's manufacturing costs [PBK10b]. This technology allows the integration of bipolar junction transistor and CMOS technology into a single integrated circuit device.

An overview of the implemented TR-modules is presented in Figure 2.7.1. It is shown that the module is mainly composed by three integrated circuits (ICs): the double balanced power amplifier (DBPA), the T/R module core integrated circuit (TRM-IC) with low noise amplifier (LNA) and phase shifter (PS), and the GaAs high isolation switch (HIS) which acts as the duplexer. While control functions and signal conditioning are dedicated to the TRM-IC [EH09a], power amplification with reduced load sensitivity is performed in the DBPA [EH09b]. The TRM-ICs have been designed to be suitable for both transmit and receive mode requirements.

The high isolation switch included in the TRM protects the receiver from damage caused by the high power of the DBPA and also serves to channel the returned echo signals to the receive path and not to the transmit path. This switching process between the transmission and reception path mush be done for the module within a time of 200 ns. The switching time is a significant value in order to satisfy the system's blind distance requirements.

Under ideal conditions, the maximum output power of one TRM at 3GHz is about 27 dBm. Consequently, this value is considered as the maximum transmit power per antenna element for the further calculation.

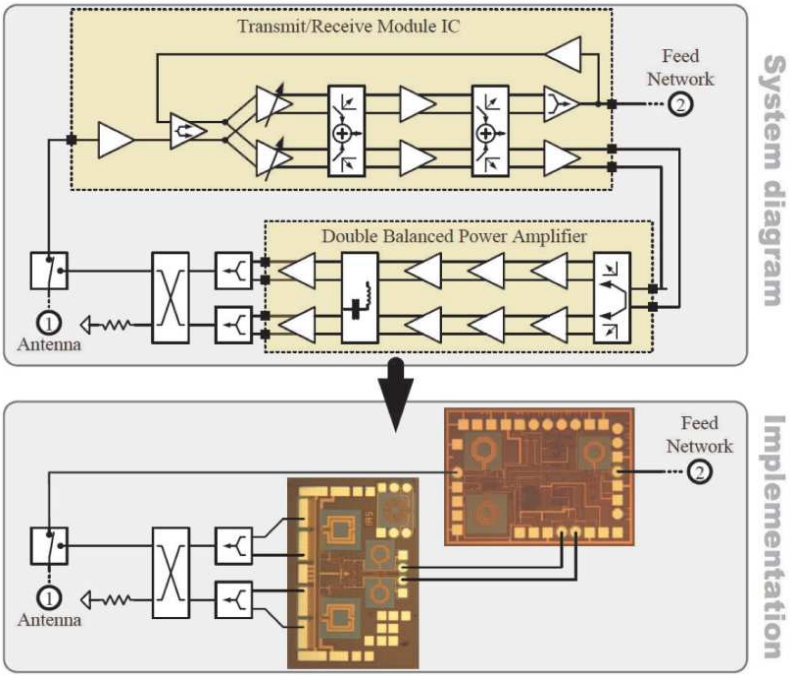


Figure 2.7.1: Block diagram of the implemented T/R module. The chip set is shown below to put in evidence the high level of integration [BPK10a].

The phased array antenna is composed of +109 elements. Each one of them has a directivity D_E that can be estimated by an ideal antenna pattern, which is composed by the E-plane pattern of an E-plane sectoral horn [Bal97] in elevation and the 3dB beam width of 120° of an active element pattern of an array antenna [Poz94] in azimuth. The directivity of one antenna element is about 11.1 dB and was obtained using a numerical integration.

Adversely to the rotating antennas, the beam of a phased array is scanned in discrete steps. For this reason it was necessary to establish the parameters of angular resolution, which define the azimuthal change of the antenna beam. As shown in [Erk09], while the minimum angle between individually detectable objects dictates the sharpness of the main beam (and therefore the number, taper and spacing of the antenna elements), the angular precision determines the minimum phase shift resolution. Requirements on the elevation were defined as a certain minimum beam width for covering an area large enough even when the platform is moving.

Table 2.7.1: Angular resolution parameters.

Minimum angular Resolution	2.5°
Angular Precision $\Delta\theta$ (Angular step size)	1°
Speed of antenna "rotation" (Refresh Time RPM)	40 $\frac{1}{min}$

The number of rotations per minute determines the d_{well} time which is the maximum time that the antenna beam spends per direction, and together with the angular antenna precision sets the minimum digital interface speed. Due to the fact that the semiconductor driven radar system employs coherent pulse integration, it is possible to affirm that the refresh time of the antenna array is the parameter that determines the maximum range as it limits the number of pulses transmitted and received per direction as is shown in Eq.2.7.1.

$$N_p^{max} = \frac{60 \cdot \Delta\theta}{RPM \cdot 360} \cdot PRF \tag{2.7.1}$$

The Radar system in development has been designed for a total distance range from 40 meters to 96 Nautical Miles (1NM = 1852m). It becomes apparent based on the parameters shown above that with a single operation mode it is not possible to cover this large range at once. Therefore the total range has been divided in three overlapping sections, which means three different operating modes called "Close", "Mid" and "Far" range.

The close range mode was designed so it has a blind distance less than 40 m and sets a coverage range of more than 1.5 NM. Due to the blind distance requirements, in this range mode no pulse compression can be used, therefore just pulse integration will be implemented. Due to the absence of pulse compression the number of sub-pulses for this mode is equal to one.

The mid range mode extends from 0.75 to 12 NM while the far range mode covers the distance from 3 to 96 NM. The blind distance restrictions for these two operational modes allow to implement not only pulse integration but also pulse compression techniques.

The number of pulses that will be transmitted for each angular step, the number of sub-pulses that compose each pulse and the pulse repetition

frequency (PRF) selected to satisfy the coverage characteristics for each one of the different operating modes are shown Table 2.7.2.

Table 2.7.2: Operating modes characterization.

Operational Mode Parameter	**Close Range**	**Mid Range**	**Far Range**
Number of Pulses N_p	108	15	3
Number of Sub-Pulses N_{sp}	100 ns	200 ns	400 ns
Sub-Pulse duration τ_{sp}	1	32	80
PRF	26.042 kHz	3.720 kHz	813.802 Hz

The noise figure of the receiver path was estimated initially as 6 dB, based on [WCM00] where for a similar X-Band system with a noise figure of 7 dB was presented. However, a more accurate approximation gives a value of 4.8 dB.

The standard performance of the system is based on a probability of detection equal to 80% and a probability of false alarm of 10^{-4}. It follows from [Sko81] and Figure 2.7.2, that under ideal conditions and weak fluctuating targets a signal-to-noise ratio equal to 11.2 dB at the receiver output after coherent processing must be available. A more realistic value equal to 14.3 dB was finally chosen to handle the possible fluctuation of the targets.

Another important parameter that was necessary to be set for the system design and calculation are the transmit/receive path losses L_{tot} which in this case have been evaluated as -14.9 dB. The individual contributions that compose the total losses are presented in Table 2.7.3. As is shown this losses include ones which are independent of the distance. However, atmospheric losses L_{atm} are a function of the distance and its value can be approximated by the factor 0.01 dB/km, at the operating frequency.

At last, in order to analyze the required transmission power for each of the different operational modes under all the above parameters and conditions, it was necessary to define certain scenarios where the radar system had to achieve the detection successfully. Most of these scenarios are defined

by [Int07]. In addition, due to the range ambiguity restrictions presented for each operational mode some other scenarios with several minimum criteria for the object detection were needed to be defined. These are shown in Table 2.7.4.

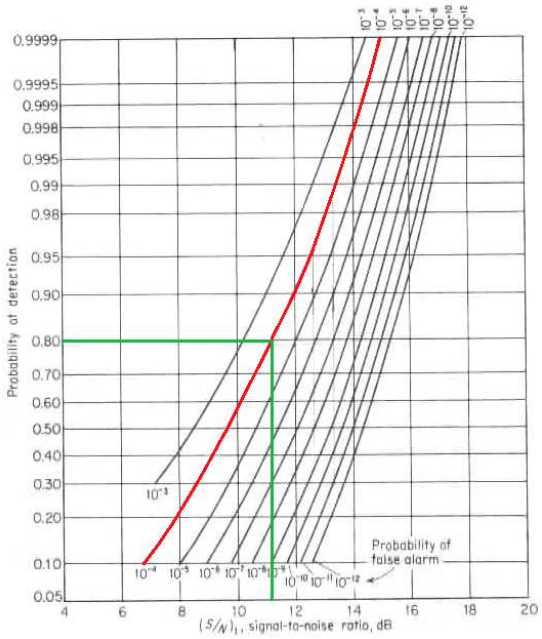


Figure 2.7.2. Probability of detection for a sine wave in noise as a function of the signal-to-noise ratio and the probability of false alarm [Sko81].

Table 2.7.3: Power dissipation estimation.

Cause of the Losses	**Transmit Path**	**Receive Path**
Radom *	- 0.5 dB	- 0.5 dB
Ohmic Losses *	- 1.0 dB	- 1.0 dB
Active Reflection Coefficient (-10dB) *	- 0.5 dB	- 0.5 dB
32 dB Taylor (4) + Quantization **	0 dB	- 1 dB
Element Pattern at 46° *	- 1.6 dB	- 1.6 dB
Weighting + Feed Network Loss**	0 dB	- 4.1 dB
Target at half-angle steps ($\Delta\theta$=1°) *		- 2.6 dB
Total Losses L_{tot}		-14.9 dB

* These represent the losses due to the antenna L_{ant}.

** These represent the losses due to the feeding network L_{feed}.

Table 2.7.4: Detection requirements.

Range [NM]	**Minimum RCS [m^2]**
1	0.1
2.625	1
3	0.5
3.6	1
3.7	0.5
8	180
11	5000
21	5000
24	5000
96	5000

Table 2.7.5 gives a summary of the most important parameters previously presented. These parameters are the essence of all the subsequent calculations.

Table 2.7.5: Global operating parameters.

Global Operating Parameter	**Value**
Carrier Frequency	3 GHz
Signal-to-Noise Ratio at the Receiver output	14.3 dB
Receiver Noise Figure	4.8 dB
Antenna Element Directivity	11.1 dB
Antenna elements per Array	109
Total Losses	-14.9 dB
Refresh Time (RPM)	40 1/min
Angular step size	1°
Atmospheric attenuation	-0.01 dB/km
Switching Time	200 ns

2.8 Operating Modes and Power Requirements

In this section, based on all the requisites and parameters previously defined, the basic calculation for the power requirements of the radar system will be performed. As already mentioned, a single operating mode is not enough to fulfill the system requirements of blind distance, radial resolution and unambiguous range simultaneously. Therefore it is necessary to check for each of the three operating modes defined in the previous section which transmission power is required to meet all the specifications within the allocated distance range. An operating mode is defined by a set of parameters, composed by Refresh time, angle step size (both constants for all the operating modes), pulse repetition frequency, number of radar pulses per angular step, number of sub-pulses and sub-pulse width of which a pulse is composed. The pulse duration can be expressed in terms of the number of sub-pulses and the sub-pulse duration as shown in Eq. (2.5.4).

The parameters that characterize each operating mode are shown in Table 2.7.1 and 2.7.2. These parameters lead to a number of derived variables that will allow to estimate the power specifications of the system. From the angular step size and the refresh time it is possible to determine the maximum time during which the array antenna, pointing in one specific direction, will be radiating the RF pulses and receiving the echo signals.

$$T_{dir,max} = \frac{60 \cdot \Delta\theta}{RPM \cdot 360} \tag{2.8.1}$$

The actual time used to face one specific direction is given by the number of pulses and the frequency with which these are transmitted and may be at most equal $T_{dir,max}$.

$$T_{dir} = \frac{N_p}{PRF} \tag{2.8.2}$$

The operating mode radial resolution depends directly on the duration of the sub-pulses that shape each pulse.

$$\Delta R = \frac{c \cdot \tau_{sp}}{2} \tag{2.8.3}$$

On the one hand, in order to determine the blind distance for the operating modes it is necessary to specify whether pulse compression is used or not. For those operating modes that implement pulse compression techniques the blind distance is determined by the time that is necessary to transmit all the sub-pulses that constitute one pulse plus the time that the T/R modules need to switch from the transmission to the reception mode.

As mentioned before the close range mode does not employ pulse compression due to the closeness of the objects to be detected and the pulse duration is smaller than in the other modes since less energy is needed. Therefore the blind distance is restricted just by the switching time of the T/R modules.

$$R_{Blind} = \begin{cases} \dfrac{c \cdot T_{Switch}}{2}, & without\ Pulse\ Compression \\ \dfrac{c \cdot (N_{sp} \cdot \tau_{sp} + T_{Switch})}{2}, & with\ Pulse\ Compression \end{cases} \tag{2.8.4}$$

On the other hand the maximum distance at which an object can be detected while a specific operating mode is being used, depends mainly on the PRF used by that particular mode.

$$R_{max} = \frac{c \cdot (\frac{1}{PRF} - N_{sp} \cdot \tau_{sp} - T_{Switch})}{2} \tag{2.8.5}$$

Based on the established parameters of the RASKEL system and the variables introduced above it is possible to characterize the different operating modes, as is shown in Table 2.8.1.

The next step is to determine the minimum transmit power per antenna element needed for each operating mode in order to satisfy the system requirements. For a linear array antenna with N_{Elem} antenna elements and with the use of the pulse shapes already introduced, the expanded radar equation [Sko81] takes the following form:

$$P_{t_{Elem}} = \frac{(4\pi)^3 \cdot F \cdot k \cdot T_o \cdot B_c \cdot R^4 \cdot \left(\frac{S}{N}\right)_{out}}{(N_{Elem} \cdot D_E)^2 \cdot \sigma \cdot \lambda^2 \cdot L_{tot} \cdot L_{atm} \cdot N_p \cdot N_{sp} \cdot N_{Elem}} \tag{2.8.6}$$

Table 2.8.1: Operating modes detailed characterization.

	Operating Mode		
Dependent Variable	**Close Range**	**Mid Range**	**Far Range**
Signal Bandwidth B_c [MHz]	10	5	2.5
Range Resolution ΔR [m]	15	30	60
Blind Distance R_{Blind} [m]	29.9792	989.3151	4826.65
Unambiguous Range R_{max} [NM]	3.0837	21.2218	96.84
Maximum d_{well} Time per Direction $T_{dir,max}$ [μs]	4166.67	4166.67	4166.67
Used d_{well} Time per Direction T_{dir} [μs]	4147.2	4032	3686.4
Duty Cycle [%]	0.26	2.38	2.60

In order to evaluate Eq. (2.8.6) it is necessary to establish a number of scenarios (combination of distances and radar cross sections) to calculate which transmit power per antenna element is needed to detect a certain target at a certain distance. These scenarios were already introduced in Table 2.7.4.

To prevent any complication due to the different ambiguity ranges of each operating mode and to reassure the overlapping between those, each mode was designed to work on a range longer than the one presented in section 2.7. For the close range mode the maximum range was designed to reach a distance equal to 1.5x1.75 NM and to be able to detect an object with a minimum RCS equal to 1 m^2. The mid range mode on the other hand had to be able to detect with the minimum transmit power per antenna element an object with 5000 m^2 of RCS at a distance none bigger than 12x1.75 NM, while the far range mode has the maximum range set at 96 NM. In Table 2.8.2 are shown the values for minimum required power per antenna element depending on the operating mode for the detection of targets at specified distances with the corresponding RCS. The empty fields in this table indicate

that the detection under the specific operating mode, distance and RCS cannot be done.

Table 2.8.2: Minimum required power per antenna element.

		Minimum Transmit Power per Antenna Element [mW]		
Range [NM]	**RCS [m^2]**	**Mode A**	**Mode B**	**Mode C**
1	0.1	102.1	11.5	
2.625 (1.5x1.75)	1	**491.6**	55.3	55.3
3	1.4	(600.9)	67.6	67.6
3	0.5	(1682.7)	189.3	189.3
3.6	1		197.3	197.3
3.7	0.5		**440.6**	**440.6**
8	180		27.7	27.7
11	5000		3.7	3.7
21 (12x1.75)	5000		53.0	53.0
24	5000			92.7
96	5000			(43875.3)

The maximum required power per antenna element calculated was 491.6 mW which represents 26.9 dBm. The T/R modules designed for this radar system are capable to provide (under ideal conditions) a maximum output power of about 27 dBm to each antenna element of the array. It is important to note that in case of the far range mode, as a target at 96 NM is impossible to detect due to the earth curvature, the minimum signal level required in this case has been neglected. Keeping this in mind it is possible to confirm that under these conditions it is possible to realize the system. In the next table the maximum distances at which the different objects can be detected are presented, if each antenna elements would radiate a power of 27 dBm.

Table 2.8.3: Maximum distance reachable to detect specific objects with a transmit power per antenna element of 27 dBm, taking into account the operating mode limitation.

	Maximum Range [NM]		
RCS $[m^2]$	**Mode A (Close Range)**	**Mode B (Mid Range)**	**Mode C (Far Range)**
0.1	1.487	2.561	2.561
0.5	2.220	3.820	3.820
1	2.638	4.536	4.536
1.4	2.868	4.929	4.929
180	3.0837	16.187	16.187
5000	3.0837	21.2218	35.477

The values of the table above illustrate the overlapping between the modes and how the ranges are clearly limited.

So far, all the parameters and variables have been presented that characterize the three operating modes and the minimum power required per antenna element so that this new radar system can assure work with extended range coverage. Now in favor of establishing all the power requirements of this system, the next step is to calculate the minimum signal and noise power level expected at the port of each antenna element due to the echoes coming from the targets. For these calculations, a power transmitted per element of 27 dBm will be assumed.

The noise power level presented at each antenna element is associated to the thermal noise and depends directly the maximum bandwidth of the receiver path. Notice that the noise power level to be calculated here by the use of Eq. (2.8.7) represents the thermal noise that is present at the input of the system transceiver when reception mode is being used. This noise will be affected by all the characteristics of the elements placed in the reception path.

$$N_o = k \cdot T_o \cdot B_c \tag{2.8.7}$$

where $k = 1.38\, x\, 10^{-23}\, \frac{J}{K}$ is the Boltzmann's constant.

$T_o = 290\, K$ is the standard room temperature.

B_c represents the Noise Bandwidth, which is approximated the bandwidth of the receiver.

Derived from the Friis transmission equation it is possible to determine the minimum received power per antenna element [Sko81].

$$P_{r_{Elem}} = \frac{P_t \cdot \lambda^2 \cdot (N_{Elem} \cdot D_E)^2 \cdot \sigma \cdot L_{ant} \cdot L_{atm}}{(4\pi)^3 \cdot R^4} \tag{2.8.8}$$

Note that as the value to compute is the received power per the antenna element, the only losses that are taken into account in Eq. (2.8.8) are from the antenna system and from the atmosphere due to the electromagnetic wave propagation. The procedure to calculate the value of minimum received power level is quite similar to the strategy applied to find the minimum transmit power.

Table 2.8.4: Minimum received power per antenna element.

		Minimum Received Power per Antenna Element [dBm]		
Range [NM]	**RCS [m^2]**	**Mode A**	**Mode B**	**Mode C**
1	0.1	-113.6	-113.6	
2.625 (1.5x1.75)	1	**-120.4**	-120.4	-120.4
3	1.4	-121.3	-121.3	-121.3
3	0.5	-125.7	-125.7	-125.7
3.6	1		-125.9	-125.9
3.7	0.5		**-129.4**	**-129.4**
8	180		-117.4	-117.4
11	5000		-108.6	-108.6
21 (12x1.75)	5000		-120.2	-120.2
24	5000			-122.6
96	5000			(-149.4)

From Table 2.8.4 and using Eq. (2.8.7) to determine the noise power level, in Table 2.8.5 are shown the minimum received signal power level and the input noise power per antenna element with respect to the different operating modes.

Table 2.8.5: Minimum received signal and noise power per antenna element.

	Mode A	**Mode B**	**Mode C**
Min. Received Signal Power [dBm]	-120.4	-129.4	-129.4
Noise Power [dBm]	-103.9772	-106.9875	-109.9978

As was mentioned before, despite the fact that the minimum received signal level is produced for an object placed at 96 NM, this values will be neglected in the course of the analysis due to the earth curvature.

Chapter 3

System Back-End

The terms "Front-End" and "Back-End" are commonly used to refer to the initial and the end stages of a radar or any radio receiver. The front-end is responsible for collecting all the different input signals and to process them in a way to match with the back-end input specifications. On the other hand, the system back-end refers to the stage where the amplification, shaping, modulation and filtering processes that accustom or refine the signal are implemented, not only for transmission but also for reception.

Concerning the RASKEL project, the radar system has been divided basically in three main stages: front-end, back-end and signal processing. The front-end is composed mainly for an RF feeding network, a large number of T/R modules and a linear array antenna of 109 identical monopoles inserted into a parallel-plate waveguide (PPW) and a horn shaped section [BPK10a]. The back-end which is the stage under analysis consists essentially of the transceiver. Therefore, it is constituted by the electronic devices that compose the transmission and reception path. At last the signal processing is a software based stage which has the aim to extract the target information from the echo signals already refined by the back-end [BPK10b].

The radar system back-end in transmission mode should generate the short duration high power RF pulses that will be radiated into space by the antenna, taking into consideration the target characteristics and the distance range where it could be located. In other words the transmitter must be able to generate the RF signal with sufficient power and the correct shape

(modulation) to perform detection for all the different operating modes. In addition, it should have RF stability to meet later the signal processing requirements, to require minimum maintenance, to be of an affordable price and to be of a reasonable size and weight for the desired application, even though no restriction for the back-end dimensions have been established.

In a different manner, the radar system working in reception mode must amplify, filter, down-convert, and digitize the echo signals in a way that it will provide the maximum discrimination between the desired echo signals and undesired interferences [Sko08]. Thus, the receiver must optimize the signal probability of detection while providing a large operation linear range. The interference comprises not only the self noise generated in the radar receiver but also the power received from galactic sources, neighboring radars and communication equipment, and jammers.

As it was mentioned earlier, this new system has been specified as a coherent radar; therefore the transmitted pulses must have defined phase angles to a reference. Whether a radar set is coherent or non-coherent always depends on the transmitter. Therefore the transmitter system that is developed in this project is of the PAT (Power-Amplifier-Transmitter) type [Wol97]. In this instance, the high-power amplifier is driven by a highly stable continuous RF waveform generator. Modulating the output corresponding to the PRF does not affect the phase of the RF source. The phase coherence is maintained even if the PRF and RF source are not locked together (RF source is phase stable).

3.1 Transceiver Design and Block Diagram

In Figure 3.1.1 the transceiver's block diagram based on all the considerations presented above has been drawn. The upper part represents the transmission path and the lower the reception path.

With the purpose of designing a coherent transmitter and assuming that the RF waveform generator is phase stable, the transmission path has been deliberately constituted by a modulation, a pulse shaping and an amplification block. The modulation block has the task of producing a simple

BPSK modulation, generating at the output a signal with alternations of 180° in concordance with a specified sequence. This modulation will be used in mid or far range mode. If the close range mode is selected, the BPSK modulator block has to let pass through the original signal without any phase changes. The pulse shaping block is called "shaping" because it controls the duration of the long pulses. It is responsible for turning on and off the RF source (already modulated). The amplification block, is the last block of the system back-end and its purpose is to supply the T/R modules and the antenna elements (System Front-End) with the correct power level, so the transmission can be carry out successfully. As all real antenna front-ends, the T/R modules have specific limitations for the signal level that they can manage at their input in order to work in linearity and to be protected of damages. Likewise these specifications will determine the power gain that is necessary in the transmission path.

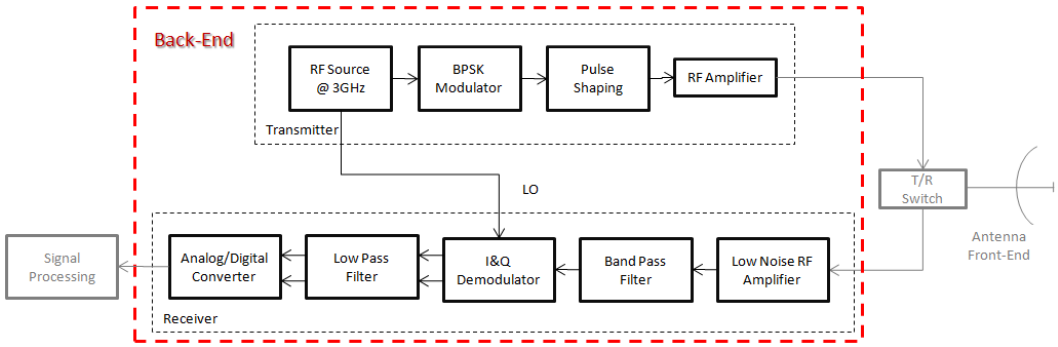


Figure 3.1.1: Back-end block diagram.

Regarding the receiver, it is important first of all to amplify the received echo signals. Since the detection range of the radar system must cover distances up to 96 NM, the expected incoming signal level may be very low. In order to achieve the amplification, it was implemented a low noise amplification block, which is placed right after the system front-end to compensate for losses in the feed line. As the noise power level is an important factor to take into consideration when it concerns the receiver design, the high gain and the position where the low noise amplifier block has been placed were selected to diminish the effect of the noise on subsequent stages of the reception path.

The band-pass filter is the next block of the reception path. Its purpose is to isolate the information signal, cancelling off all the other frequency components at higher and lower frequencies that could add strong interferences. This filter, due to the fact that the I&Q demodulator is an active component, will also cancel other frequencies components that can be generated at its output. The next stage consists of the I&Q demodulator. This block applies a smart approach for separating the real and imaginary part of the received complex signal without losing essential information. As a local oscillator signal is needed for the I&Q demodulator it has been chosen the signal generated in the transmitter by the RF source, so it would be possible to obtain at the outputs the baseband in-phase and quadrature components of the received echo signals. Following that, it has been placed a low-pass filter block to remove all the high frequency components that could cause interference and to prevent aliasing during the sampling that will be executed by the last stage of the receiver path.

Finally the block that completes the reception path, and consequently the system back-end, is the analog-to-digital converter. This block is in charge of the digitization of the in-phase and quadrature components of all the received echoes, which will be transmitted to the radar signal processing stage where they will be analyzed. The ADC limits the linear dynamic range of the whole receiver. This block is particularly critical in the reception path due to the fact that it forces some specific power characteristics that the incoming signal must satisfy in order to achieve a correct signal processing. These requirements, together with the conditions of noise figure and signal-to-noise ratio at the input of the signal processing stage limit the behavior of the receiver, allowing to estimate the gain that is necessary to supply along the reception path.

3.2 Low Cost Transmitter/Receiver Innovation

The RASKEL project has as an aim to study the feasibility of construction of a new radar system that tries to introduce many different innovations to the conventional ship-born navigation and coast surveillance systems that have been operated until the present day. The feasibility of the

whole system depends on the antenna front-end. Although the most critical and innovative components concern the system front-end design and construction, some refinements have been contemplated for the system back-end as well.

The system back-end is an RF unit whose innovation consists basically in the employment of low cost commercial components off the shelf (COTS) in its construction. COTS components are commonly used for wireless communication system and wireless LAN. These components have been successfully used to replace the traditional (custom) system for radar, sonar, telecommunications and missile guidance applications, and others. Commercial off the shelf (COTS) is a term used as evidence of the technology which is ready-made and available for sale, lease or license for the general public. The use of COTS components has been recommended by several governments and business programs due to the fact that their implementation may offer significant savings in procurement, development and maintenance.

As said before, the incentives for using COTS components include mainly the hope for a considerable reduction of the overall system development time, costs and long-term maintenance. However, their usage results in some disadvantages that affect the system, especially in the design process. The COTS components are produced in large quantities, and have been designed for a general purpose that may not be suitable for all applications, in this case design and construction of special component is necessary with a highly deterministic performance.

Nevertheless, the use of COTS components has great potential in the area of network systems [IA99] and also for the construction of this particular system back-end due to the simplicity of the tasks for which they are needed. The system back-end's high dependability on COTS hardware makes its design cost-effective, collaborating in this way to satisfy the low-cost premise established in the RASKEL project.

Chapter 4

Power Level Plan

The power level plan is undoubtedly an indispensable tool for the design and analysis of hardware-based systems. The term power level plan (PLP) refers to the power analysis performed on a specific signal path where the signal and noise power level existing at its input will be modified by the characteristics of the different elements that are placed throughout this path. This evaluation considers several characteristics of the elements that belong to the signal path e.g.: gain, noise figure, input and output power requirement and linearity range. In this section, together with an estimation of the total gain required along the transmission and reception path, it will be executed the evaluation of the signal and noise power level ratio at all the different points of these signal paths.

4.1 Estimation of Receiver Gain and Linear Dynamic Range

As mentioned in the section 3.1, the ADC is the most important element of the reception path as the linear dynamic range depends strictly on this element. At the output of this device the digitized in-phase and in-quadrature components of the echo signals must be available, which are required to have a SNR at least equal to 14.3 dB. The A/D converter makes the transformation between the continuous signal and the digital domain. As

the receive path is based on the continuous signal domain it is necessary to refer the signal requirements at the input of the ADC instead of its output. The relations of the signal and noise power level at the input of the ADC are illustrated in the Figure 4.1.1. From this it is possible, in the case of reception, to attribute to the system an overall gain, a maximum total noise figure and the linear dynamic range of the A/D converter input [Ber07a].

The selected model of the A/D converter that has been chosen for the prototype construction will be formally introduced in the Chapter 5. However for the calculations presented in this section it is just necessary to consider the following features of the ADC board.

- Resolution (NB_{ADC}): 14 bits.
- Effective Number of Bits (ENOB): 11 bits.
- Input Impedance (Z_{in}): 50 Ω.
- Input Voltage Range: from -1 to +1 V.
- Number of channels (N_{CH}): 2.

All these values have been selected based on a similar analysis shown in [Ber07a].

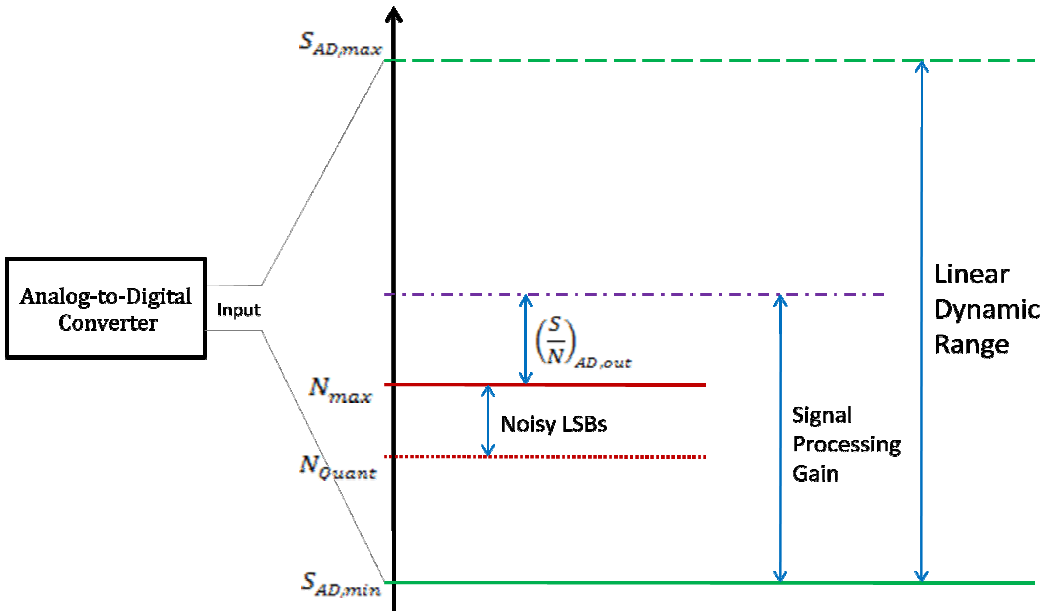


Figure 4.1.1: Signal and noise power level at the A/D converter input [Ber07a].

The starting point of the characterization consists in finding the maximum input signal power level that the ADC board can handle while it is still working in the linear range. This value corresponds to the average signal power level. The echoes received by the system front-end are RF signals and have been, so far, referred to theirs average signal and noise power levels. For this reason the power and noise requirements of the ADC have been also referred to the average power level instead of the peak power level.

$$S_{AD,max} = \frac{U^2}{2 \cdot Z_{in}} \tag{4.1.1}$$

where Z_{in} is the input impedance and U is the maximum input voltage.

The following estimation is the signal-to-quantization-noise ratio (SNRq). As a full scale sine wave is the wave form of the input signal, the quantization level approximates a saw tooth wave with peak amplitude of one quantization level and uniform distribution. Using Eq. (4.1.2) it is possible to estimate the SNRq in dB.

$$\left(\frac{S}{N}\right)_{Quant}[dB] = ENOB \cdot 6dB + 1.8dB \tag{4.1.2}$$

It is important to remark that the approximation for the signal-to-quantization-noise ratio is conventionally established with the resolution of the analog-to-digital converter instead of just the ENOB as shown in Eq. (4.1.2). However for these calculations the ENOB have been used in order to work with the effective number of bits which contain useful information and have not been affected by the noise floor of the A/D converter.

Having the two previous values it is accessible to find the quantization noise power:

$$N_{Quant} = \frac{S_{AD,max}}{\left(\frac{S}{N}\right)_{Quant}} \tag{4.1.3}$$

The maximum expected signal noise power at the A/D converter input should be about two bits higher than the quantization noise so that the subsequent coherent signal processing techniques (applied after the ADC) will work effectively.

$$N_{max}[dB] = N_{Quant}[dB] + 2 \cdot 6dB \tag{4.1.4}$$

Finally it is possible to determine the minimum signal power level at the A/D converter input. This value is different for each of the operating modes as it depends directly on the used number of pulses and sub-pulses.

$$S_{AD,min} = \frac{\left(\frac{S}{N}\right)_{AD,out} \cdot N_{max}}{N_p \cdot N_{sp}} \tag{4.1.5}$$

where $\left(\frac{S}{N}\right)_{AD,out}$ is the signal-to-noise ratio after the coherent signal processing (at the ADC output).

Knowing the minimum ADC input signal power level and the minimum received power per antenna element listed in Table 2.8.5, it is permitted to estimate the necessary signal gain that must be supplied to the back-end receive path.

$$G_{Rx,signal} = \left(\frac{S_{AD,min}}{P_{r\,Elem}}\right) \tag{4.1.6}$$

The feeding network used for the array antenna consists in a passive structure which sums coherently the signals received by all the antenna elements, while the noise power level received per antenna element is summed incoherently. This structure provides in this way a better SNR due to the amplified signal power level. As a result the signal gain and the noise gain are not equivalent, being the noise gain lower by a factor N_{Elem}.

$$G_{Rx,noise} = \frac{G_{Rx,signal}}{N_{Elem}} \tag{4.1.7}$$

It is important to verify if the level of noise at the ADC input satisfies the 2 bits condition established at the beginning of the ADC characterization. The following expression estimates the ADC input noise from the thermal noise received at the antenna front-end. Notice that as Eq. (4.1.8) calculates a noise power level, it uses the noise gain instead of the signal gain.

$$N'_{max} = \frac{k \cdot T_o \cdot B_c \cdot F \cdot G_{Rx,noise}}{L_{feed}} \tag{4.1.8}$$

where L_{feed} represents the losses due to the feeding network.

The feeding network losses and the receiver noise figure were considered separately by the previous formula as they have also been considered in this way during the radar equation demonstration shown in section 2.2. In addition, not considering the feeding network losses due to the tapering used in reception inside the total losses made simpler the procedure to find the received signal power level per antenna element.

It is necessary to check with Eq. (4.1.9) if at least the required value of signal-to-noise ratio at the ADC output has been reached with the previous estimated receiver gain G_{Rx}.

$$\left(\frac{S}{N}\right)'_{AD,out} = \left(\frac{S_{AD,min}}{N'_{max}}\right) \cdot N_p \cdot N_{sp} \tag{4.1.9}$$

In order to finish the ADC characterization, it is necessary to calculate the minimum memory needed for the ADC for accumulating all the samples obtain during the scan in one direction.

$$Memory_{x\ direction} = \frac{R_{max}}{\Delta R} \cdot N_p \cdot N_{CH} \cdot NB_{ADC} \tag{4.1.10}$$

where N_{CH} is the number of channels used by the ADC and NB_{ADC} is the ADC resolution.

As the radar system is composed by 4 system modules as shown in Figure 2.6.2, and each one of them has an angle-range of 90°, the minimum memory needed for one of the modules used in this radar system can be calculated multiplying the previous value by a factor equal to 90 divided by the angular step size.

$$Memory_{total\ scan} = Memory_{x\ direction} \cdot \frac{90°}{\Delta\theta} \tag{4.1.11}$$

The results of all the previous calculation steps are shown in Table 4.1.1.

Having in mind the variables above, it is simple to estimate the linear dynamic range of the ADC, which consists basically in the relation between the maximum and the minimum A/D converter input power.

$$LDR = \left(\frac{S_{AD,max}}{S_{AD,min}}\right) \tag{4.1.12}$$

Table 4.1.1: Analog-to-digital converter characterization.

	Operating Mode			
Variable	**Close Range**	**Middle Range**	**Far Range**	**Units**
ADC Maximum Input Signal Power $S_{AD,max}$	10			dBm
SNRq $\left(\frac{S}{N}\right)_{Quant}$	67.8			dB
Quantization Noise Power N_{Quant}	-57.8			dBm
ADC Maximum Input Noise Power N_{max}	-45.80			dBm
ADC Minimum Input Signal Power $S_{AD,min}$	-51.83	-58.31	-55.30	dBm
Reception Path Signal Gain $G_{Rx,signal}$	68.57	71.09	74.10	dB
Reception Path Noise Gain $G_{Rx,noise}$	48.19	50.71	53.72	dB
ADC Input Noise Power N'_{max}	-45.89	-46.37	-46.37	dBm
ADC output SNR $\left(\frac{S}{N}\right)'_{AD,out}$	14.39	14.87	14.87	dB
Linear Dynamic Range	61.83	68.31	65.30	dB
Minimum Memory needed per Direction	1.15	0.55	0.25	Mbits
Minimum Memory needed per Angle Range	103.69	49.56	22.62	Mbits

The feeding network as well as the ADC, are some of the critical parts of the system, especially when it concerns the analysis of the signal and noise

power levels. A power divider is commonly employed as feed network, as it delivers the same RF power to all T/R Modules, these have to cover a wide amplitude tuning range for proper illuminating tapered arrays. Tapering is mandatory in any highly selective radar system [Erk09]. A phased array can achieve high side-lobe suppression levels by varying the magnitude of the weights connected to each one of the antenna elements. Usually, the antenna element placed in the center of the array can transmit and receive with all the power while an attenuation is applied to the surrounding elements. Tapering the receiver illumination is essential for compliance with the specified antenna diagram.

For this particular system the project partners proposed a new feeding network which is compact and "lossless" [Ber07c]. This feeding network will contribute to achieve the selected receive antenna tapering α_m that consists in a Taylor distribution with a peak-sidelobe level of 32 dB and the first four sidelobes with the same amplitude levels, decaying rapidly in amplitude afterwards [Erk09]. As the feeding network is a lossless passive structure, it has been designed so it can always provide a square root Taylor distribution. In reception mode, the tapering of the array is made by the T/R-modules, which have to convert their signals also to a square root Taylor distribution, so in combination with the feeding network it will be possible to generate the desired Taylor receiving antenna pattern. A schematic representation of the feeding network used in the receiver is illustrated in Figure 4.1.2.

In Figure 4.1.2 the T/R modules are represented by the active element with gain $G_{amp} \cdot A_m$. The parameters A_m represent the attenuation that must be software-selected in the T/R-modules with a square root Taylor distribution. On the other hand, the parameters B_m correspond to the fixed attenuations present in the feeding network with the same distribution as the coefficients A_m. The desired tapering is created by the product of the power scaling parameters A_m and B_m. The parameters A_m have been normalized so the center element of the array has an attenuation of 0 dB. However, as the feeding is based on the use of a power splitter which involves and attenuation of $1/N_{Elem}$, to satisfy the previous statement of a lossless passive structure, the power conservation principle (the power level at its input must correspond to the power level at its output) has to be considered. Therefore, the parameters B_m are normalized considering a scaling factor f that

compensates this extra attenuation. The f factor is defined in the following way:

$$\sum_{m=1}^{N_{Elem}} \frac{B'_m}{N_{Elem}} \cdot f = 1 \tag{4.1.13}$$

Being the definitive B_m coefficients given by the Eq. (4.1.14)

$$B_m = f \cdot B'_m \tag{4.1.14}$$

where: B'_m coefficients correspond to a square root Taylor distribution with an arbitrary scaling.

N_{Elem} is the number of elements of the array.

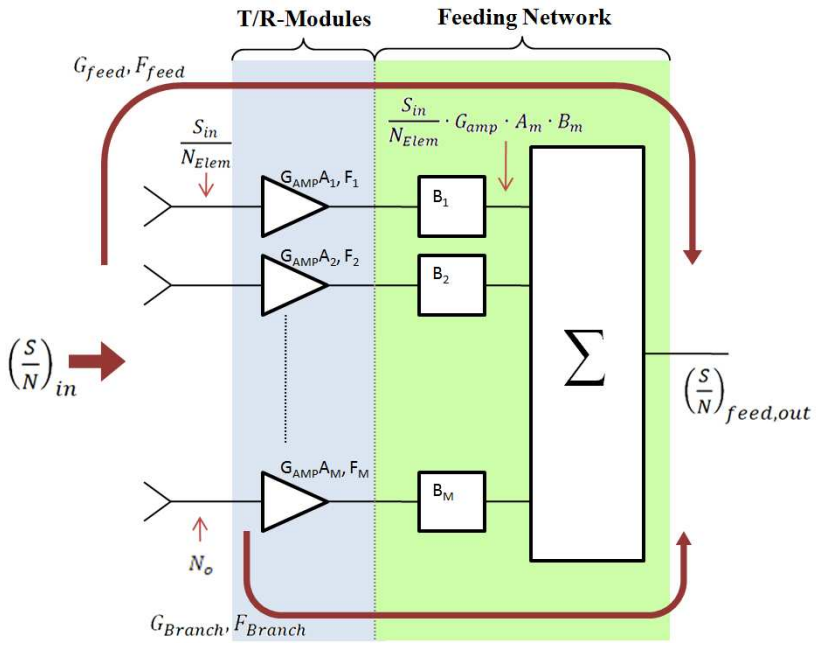


Figure 4.1.2: Schematic representation of the feeding network in reception mode.

As the feeding network is a passive structure, losses will be involved. An attenuation of 3 dB per branch included in the B_m coefficients has been considered for the matters of this design. The total losses due to the tapering can be calculated as follows:

$$L_{feed} = \frac{\left(\sum_{m=1}^{N_{Elem}} \sqrt[2]{A_m \cdot B_m}\right)^2}{N_{Elem}^{\ 2}} \tag{4.1.15}$$

These losses correspond to the estimated 5.1 dB of losses due to the feeding network that were considered in Table 2.7.3. The shape of the Taylor distributed tapering used in reception mode is shown by Figure 4.1.3.

Keeping in mind Figure 4.1.2 and considering one individual antenna element (one branch of the network), the gain and noise figure of the feeding network can be defined. These quantities are important for setting up the complete power level plan of the reception path. However, determining gain and noise figure of the feeding network in case of aperture tapering is not straight forward.

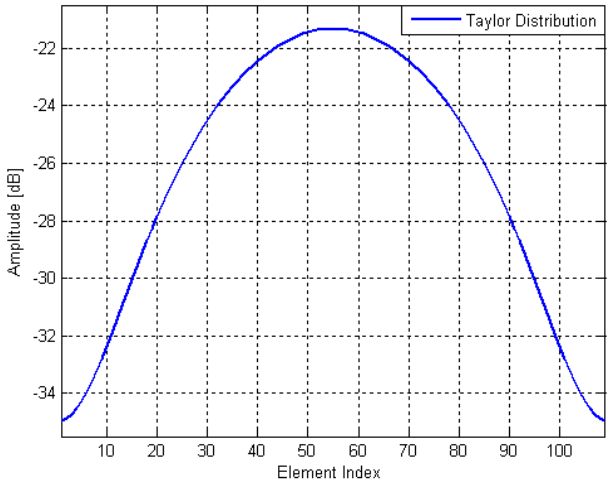


Figure 4.1.3: Tapering distribution used in reception mode.

At the feeding network's common port, the received radar signals add up coherently [GDS04]. From the coherent summation of all the signal power received by the elements of the array the gain related to the feeding network can be found as shown in Eq. (4.1.16).

$$G_{feed} = \frac{1}{N_{Elem}^2} \cdot G_{amp} \cdot \left(\sum_{m=1}^{N_{Elem}} \sqrt{A_m \cdot B_m}\right)^2 \tag{4.1.16}$$

Differently the gain seen by only one of the feeding network branches will be bigger by a factor N_{Elem} as the received power by one antenna element is being massively increased when it is referred to the output of the feeding network where the signals coming from all the different branches have been coherently summed.

$$G_{Branch} = N_{Elem} \cdot G_{feed} \tag{4.1.17}$$

On the other hand the noise contributions from the different antenna elements are uncorrelated, thus are incoherently summed [GDS04]. Considering the 2-Port network with a specific gain G and noise figure F as shown in Figure 4.1.4 the signal and noise power at the output can be calculated using Eq. (4.1.18) and Eq. (4.1.19), respectively.

$$S_2 = G \cdot S_1 \tag{4.1.18}$$

$$N_2 = G \cdot [N_1 + N_o \cdot (F - 1)] \tag{4.1.19}$$

where: S_1 and S_2 are the signal power levels at the input and output of the 2-port network, respectively.

N_1 and N_2 are the noise power levels at the input and output of the 2-port network, respectively.

Figure 4.1.4: Schematic representation of a 2-port network.

Now, recalling Eq. (2.3.2), it can be rewritten as:

$$F = \frac{\left(\frac{S_1}{N_1}\right)}{\left(\frac{S_2}{N_2}\right)} \tag{4.1.20}$$

which is valid if and only if $N_1 = N_o$, where N_o represents the thermal noise. In case of $N_1 \neq N_o$, the correct expression is given by Eq. (4.1.21).

$$F = \frac{\left(\frac{S_1}{N_1}\right)}{\left(\frac{S_2}{N_2}\right)} - \frac{N_1}{N_o} + 1 \tag{4.1.21}$$

Combining Eq. (4.1.20) and (4.1.19), it is easy to calculate the noise power level at the output of the feeding network.

$$N_{feed,out} = \frac{N_o}{N_{Elem}} \cdot \left[G_{amp} \cdot \left(\sum_{m=1}^{N_{Elem}} A_m \cdot B_m \cdot F_m \right) + N_{Elem} - \sum_{m=1}^{N_{Elem}} B_m \right] \tag{4.1.22}$$

Regarding the calculations of the noise figure (F_{feed} and F_{Branch}), these values were found using again Eq. (4.1.20). However, it is important to remark that after the measurement of the T/R-modules the noise figure has been approximated obtaining as a result the noise figure distribution illustrated in Figure 4.1.5. Observe how the noise figure value of each T/R-module depends strongly of its particular gain ($G_{amp} \cdot A_m$).

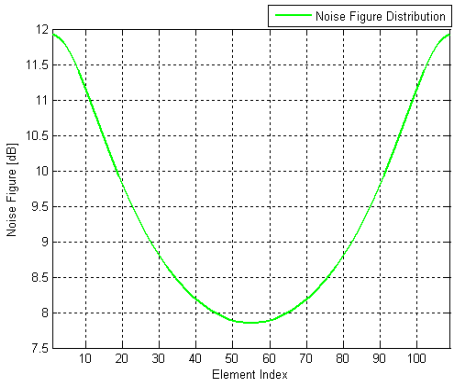


Figure 4.1.5: T/R-modules' noise figure distribution.

4.2 COTS Based Receiver

Until this point the system Back-end has been designed and projected on a theoretical basis. To check whether the system design using

commercially available components (COTS) is practically possible or not, an exemplary power level plan must been done first, using as reference actual commercial devices that may be bought later to build the prototype if they satisfy the system requirements. The power level plan shown in this section consists, in fact, in the definitive PLP of this system's back-end. This mean that the component features exhibited along this section symbolize the final devices that were selected, bought or designed especially for the assembly. However these components will be formally introduced in Chapter 5.

The COTS selected are often used in the field of mobile telephone or wireless LAN. The reason of their selection is that these components must assist the system back-end to achieve by coherent signal processing (A/D converter) a signal-to-noise ratio of at least 14.3 dB. As the system operates in three different modes the minimum signal power level at the ADC input, in all the cases, may exceed the absolute minimum value calculated in the previous section. However this excess must not be too large, otherwise the linear dynamic range would be also reduced.

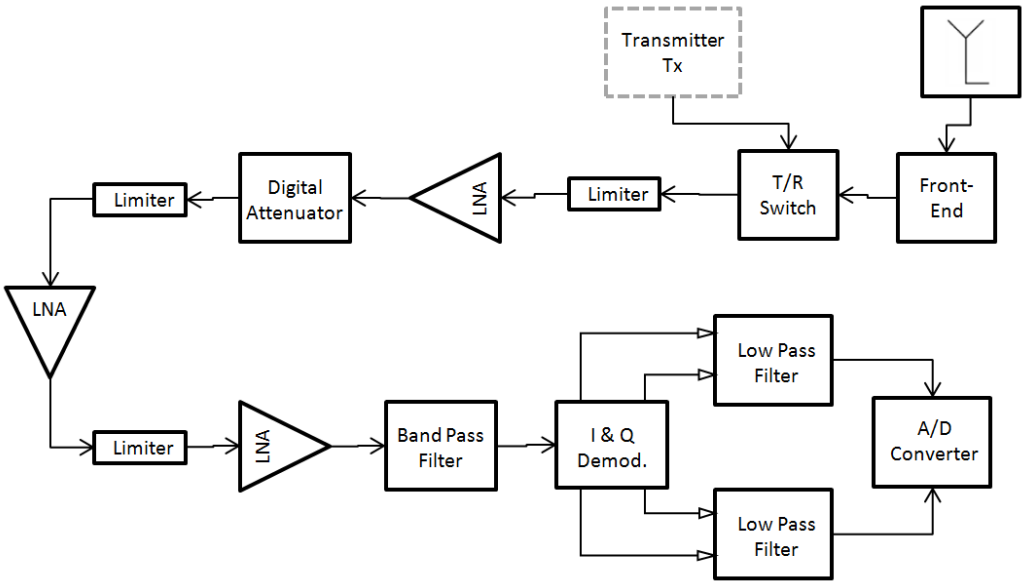


Figure 4.2.1: COTS Based Receiver Block Diagram.

Considering that an extensive search for suitable electronic devices preceded the selection of the components, the block diagram shown in

Chapter 3 had to be improved in order to consider a more realistic model of the system. Notice that along the reception path were included three limiters that were placed right before each LNA. This has been done with the intention of protecting the low noise amplifiers from exceeding their maximum input power under any circumstances, so these devices and the receiver in general will not suffer any damage.

As the use of commercial COTS low noise amplifier allows to reach just certain gains, an digital attenuator was included in the reception path in order to provide for each operating mode the closest upper value of signal gain respected to the estimated values shown in Table 4.1.1. This has been done also to optimize the linear dynamic range of the system. The position of this particular component was also decisive as it is necessary to assure the linear behavior of all the components along the reception path within the linear dynamic range of the ADC. Therefore, in order to avoid that the second and third LNAs go in saturation before the ADC, limiting in this way the linear dynamic range of the whole receiver, the digital attenuator had to be placed after the first LNA instead of later on the reception path. The high noise figure given by the digital attenuator does not really affect the receiver noise figure due to the high gain given by the first LNA and the feeding network where all signal contributions from the antenna elements have been coherently summed up.

In Table 2.8.1 are shown the signal bandwidths for the three operating modes used in this system. It is natural to assume that a specific low pass filtering must be done depending of the mode in which the radar system is working. However, due to the fact that the signal processing stage of this radar system will apply a digital low pass filtering with a specific bandwidth for each operating mode, the low filter placed in the reception path has been selected so it can filter all the different echo signals regardless of the operating mode. Due to this fact, its bandwidth corresponds to the bandwidth of the signal used by the close range mode.

On the other hand the sampling rate of the ADC should also change depending on the operating mode in use. However a down sampling will be applied after the coherent signal processing as well, so the sampling rate of the ADC is fixed and remains invariable.

As the stage composed by the I&Q demodulator is characterized by the output voltage range and the ADC has a limited input voltage range, the used low pass filter has been designed in order to match both ranges. The formal presentation of the active differential input/single-ended output low pass filter designed for this system will be done in Chapter 5. Considering that this filter will allow all the voltage values given at the I&Q demodulator output to be perfectly filtered and received at the ADC input within its voltage range, it is necessary, in order to assure the reception process without bringing the ADC to saturation, that the maximum signal power level at the ADC input matches the maximum signal power level at the I&Q input port. As a result, for the matter of the power level plan will be assumed that the I&Q demodulator and the low pass filter behave linearly and they both have a gain of 0dB. Regarding the noise figure of these stages, it is obvious that no matter how high are their magnitudes, as these components are placed at the end of the receiver chain, their noise contribution will be negligible due to the high signal gain supplied by the earlier stages.

In Table 4.2.1 are listed the measured values of gain and noise figure respective to the receiver COTS. The gain and the noise figure of the feeding network were calculated on basis of the considerations presented in section 4.1 and [VDS04].

Considering the cascaded system shown in Figure 4.2.2 where each component has its specific gain G_m and noise figure F_m the total noise figure of the whole system in given by:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} + \frac{F_4 - 1}{G_1 \cdot G_2 \cdot G_3} + \cdots \qquad (4.2.1)$$

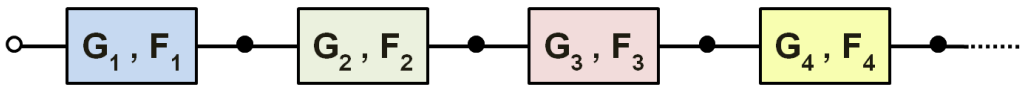


Figure 4.2.2: Schematic of a cascade system.

Table 4.2.1: Measured characteristics of the receiver path stages.

Stage	**Component**	**Gain [dB]**			**Noise Figure [dB]**		
		Mode A	**Mode B**	**Mode C**	**Mode A**	**Mode B**	**Mode C**
1	Antenna *	0			0		
2	Transition *	-0.5			0.5		
3	IAS- HL- Feeding Network *	39.329			-11.0496		
4	T/R Switch	-1.5			1.5		
5	Power Limiter n°1	-0.38			0.394		
6	LNA n°1	17.79			3.085		
7	Digital Attenuator	-18.34	-15.72	-12.75	18.364	15.8105	12.768
8	Power Limiter n°2	-0.38			0.391		
9	LNA n°2	17.79			3.075		
10	Power Limiter n°3	-0.41			0.418		
11	LNA n°3	17.71			3.127		
12	Band-Pass Filter	-2.347			2.343		
13	I&Q Demodulator	0			14		
14	Active Differential Low-Pass Filter	0			10		
Total		68.758	71.448	74.353			

* System front-end components whose values were given by [Ber07a] and not measured.

In spite of the fact that the receiver is a cascade system, Eq. (4.2.1) cannot be used to calculate the noise figure of the entire receiver as it is necessary to consider the losses due to the feeding network and the effects of the coherent signal processing. For this system it is necessary to use Eq. (4.2.2) to calculate the receiver noise figure (from the array antenna aperture until the ADC output) for each operating mode. Here the SNR at the ADC output is expressed as the SNR before the signal processing divided by the number of pulses and sub-pulses due to the pulse integration and pulse compression techniques used in this radar system, while the SNR at the array antenna port is shown as the SNR of a single antenna element multiplied by the number of elements. The results of the signal-to-noise ratio, linear dynamic range and the total receiver noise figure for each operating mode are presented in Table 4.2.2.

$$F = \frac{\left(\frac{S}{N}\right)_{ant}}{\left(\frac{S}{N}\right)_{ADC,out}} \cdot N_p \cdot N_{sp} \cdot N_{Elem} \cdot L_{feed} \qquad (4.2.2)$$

Table 4.2.2: SNR after coherent signal processing, receiver linear dynamic range and receiver noise figure for all the operating modes.

Operating Mode	**$SNR_{ADC,out}$ [dB]**	**LDR [dB]**	**Receiver's NF [dB]**
Close Range	14.422	61.642	4.819
Mid Range	14.922	68.018	4.807
Far Range	14.929	65.047	4.800

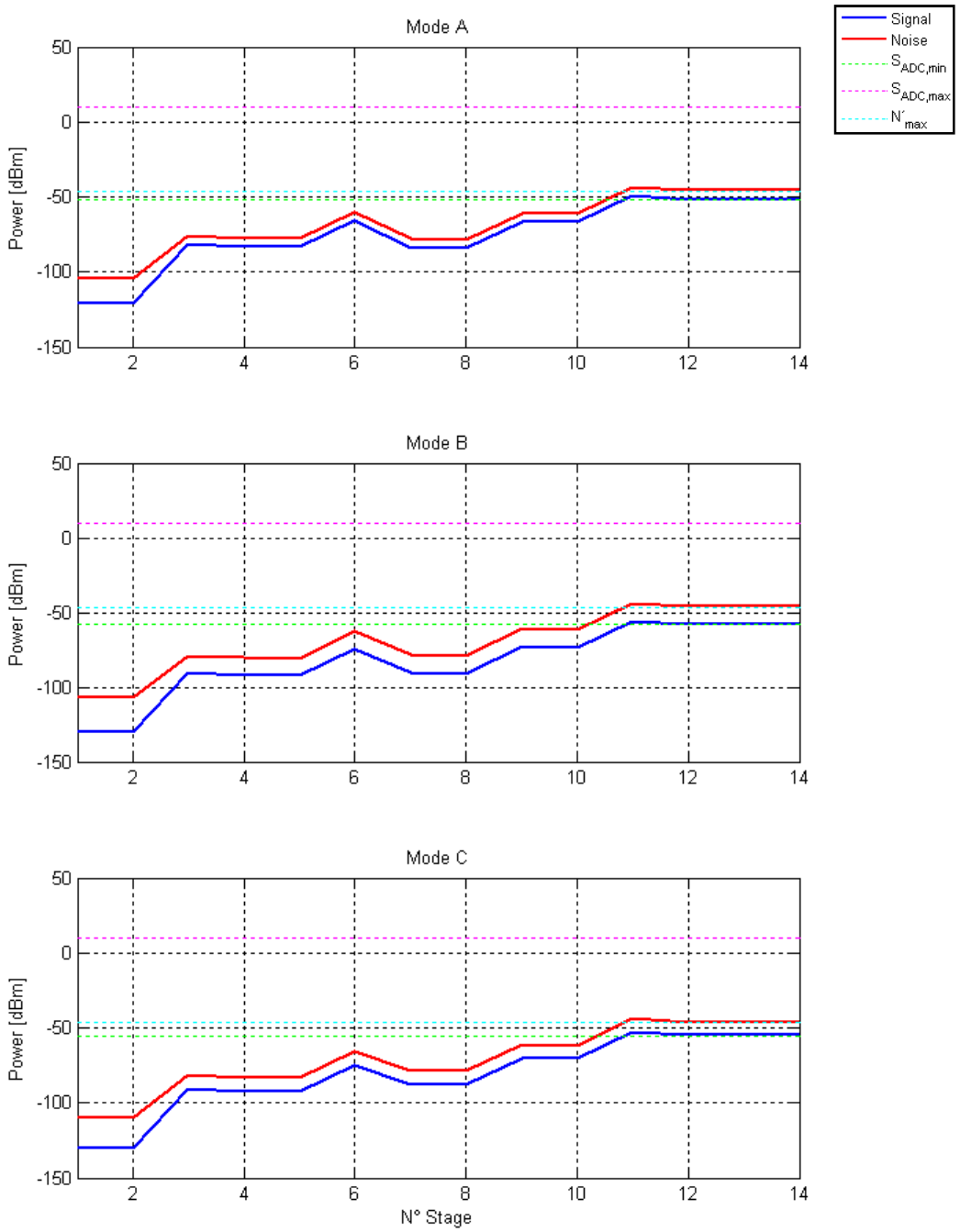


Figure 4.2.3: Signal and noise power level for the three operating modes.

In Figure 4.2.3 the results of the power level plan for the reception path have been illustrated. It shows the curves of the signal and noise power level along the receive path for the three operating modes. The level at stage

one corresponds to the output of the antenna element whose value of signal and noise power level was fixed in concordance with Table 2.8.5, so the value of signal power expected represents the worst case. It can be observed that the poor signal-to-noise ratio changes at the stage 3 (feeding network), where it is shifted to a value that remains constant for the rest of the reception path. This value is related to the subsequent coherent signal processing (A/D converter) where the SNR desired will be achieved due to the pulse integration and pulse compression techniques.

As was mentioned before, the programmable attenuator was used to fix the minimum signal power level at the ADC input to the minimum value possible, so the ADC will make profit of the use of its entire linear dynamic range.

In Figure 4.2.4 is shown the minimum signal-to-noise ratio at each individual level with respect to the required SNR after coherent signal processing. It is clearly presented by this figure that the required value of signal to noise ratio is achieved just after the coherent superposition of the feeding network. As is shown by this figure and Table 4.2.2 all the requirements of SNR and noise figure established in Chapter 2 have been satisfied.

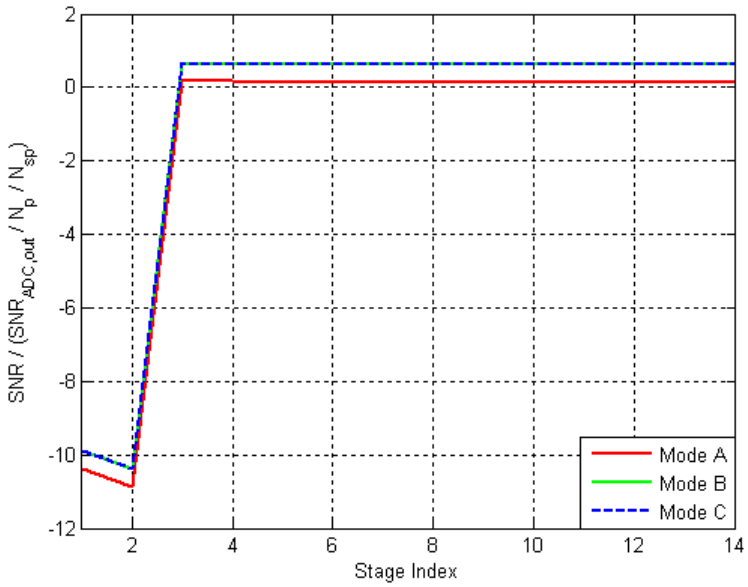
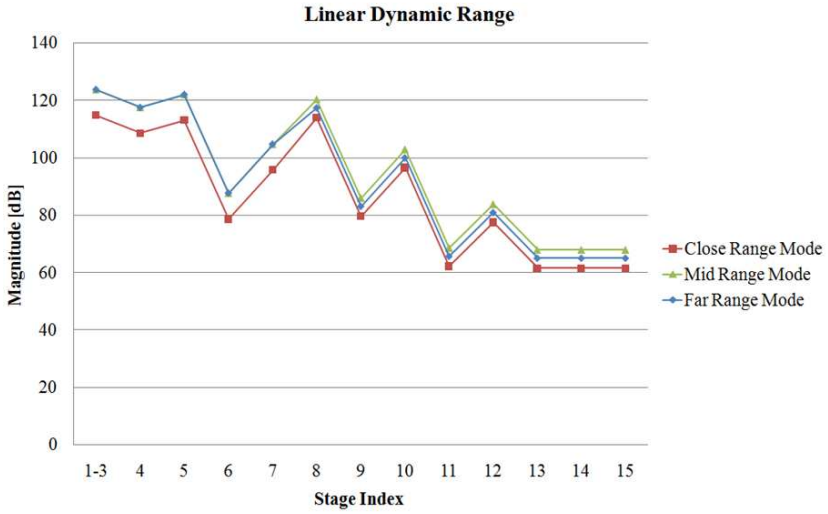


Figure 4.2.4: Minimum signal-to-noise ratio at each individual level with respect to the required SNR after the coherent signal processing.

Finally, in order to confirm that the system can be build based on these components, has to be considered one more detail. The saturation of the individual components has to be verified, as the receiver's entire dynamic range could be limited by them. This analysis has also the aim to examine each component's power limitations, so none of them suffers any damage.

The next figure shows the different linear dynamic ranges of all the components that constitute the receiver specifying the operating mode. All the dynamic ranges have been determined by the respective mode's minimum input power level (worst case) and the maximum input power of each stage. For those components that present a linear operation range, the input 1 dB compression point has been considered instead of the simple maximum input power that they can handle. The goal of this analysis is to verify if all the selected components placed along the reception path operate in linearity at least while the ADC works in its linear dynamic range. The stages one to three were put together as all these components belong to the system front-end.



Stage	Component
1	Antenna
2	Transition
3	IAS- HL- Feeding Network
4	T/R Switch
5	Power Limiter n°1
6	LNA n°1
7	Digital Attenuator
8	Power Limiter n°2
9	LNA n°2
10	Power Limiter n°3
11	LNA n°3
12	Band-Pass Filter
13	I&Q Demodulator
14	Active Differential Low-Pass Filter

Figure 4.2.5: Linear dynamic range of the receiver components.

The linear dynamic range of the receiver is given by the component with the smallest linear dynamic range. Notice in Figures 4.2.5 how the linear dynamic ranges of all the components are bigger than the one of the analog-to-digital converter. Therefore the hypothesis previously made, where was

taken for granted that the ADC board was the component that limited the linear dynamic range of the whole receiver was true. Observe also how the fact of placing the digital attenuator after the first LNA to decrease the signal power level at the input of the second and third LNAs increased their linear dynamic range avoiding them to be smaller than the one of the ADC. Not placing the digital attenuator in this position will saturate the second and third LNA with an input signal power level lower than the one needed to saturate the ADC, reducing consequently the linear dynamic range of the whole receiver.

Knowing the linear dynamic range of each one of the components of the receiver, it is possible to establish the maximum input signal power level of the whole receiver. This parameter indicates the maximum input signal power level per antenna element that allows us to assure that the receiver is still working in linearity. In other words, any other input power level per antenna element higher than this value will saturate at least one of the components of the receiver. The detection process, under these conditions, will not be linear anymore. This value is determined, in this particular case, for the maximum input power level of the last stage of the receiver path (ADC) and its total gain.

Table 4.2.3: Receiver's maximum input signal power level.

Operating Mode	**Maximum Input Signal Power Level [dBm]**
Close Range	-58.76
Mid Range	-61.38
Far Range	-64.35

4.3 Estimation of Transmitter Gain and Linear Dynamic Range

For the power level plan of the transmitter just the signal power level analysis of the system will be executed. As the noise power generated at the transmitter does not affect the noise floor received by the antenna in

reception mode, it is not necessary to fix the noise level to a certain level. However the transmitter must be able to generate a very stable signal, where the different pulses and sub-pulses present a much defined shape with the enough RF power.

As well as with the receiver case the feeding network is a critical part of the system design. In transmission it is important to generate the signal with sufficient, but not too high power that feeds at each T/R Module and with stable and reproducible phase. Which phase exactly is presented at the T/R module is not relevant, as the phase will be corrected by them.

No aperture tapering or unity illumination is used in transmission mode. Recalling that the feeding network has been designed to have a square root Taylor distribution, no tapering is realizable if all the T/R-modules operate with saturated output power. If the amplifiers contained in the T/R-modules are saturated, the output power of all the antenna elements will be the same and equal to $S_{sat.}$. Therefore, the power distribution given by the feeding network will not be effective anymore. An equivalent schematic of the feeding network working in transmission mode in shown in Figure 4.3.1.

In order to estimate the gain needed in the transmission path it is necessary first of all to know the input power that has to be given to the feeding network, so regardless of the unavoidable square root Taylor distribution it is possible to saturate all the T/R-modules. In order to deliver a saturated output power from all the T/R-modules and at the same time without damaging them, each one of these modules must be fed with a signal power level between -5 and -15 dBm.

In Figure 4.3.2 the tapering applied in transmission including 3 dB of estimated losses has been illustrated, showing all the specific attenuations per antenna element. Observe that the dynamic range of the square root Taylor distribution is about 6.8 dB. Considering now the tapering used and the power requirements of the T/R modules, it is very straightforward to establish a power condition at the system back-end output in order to satisfy the power demands of all the modules. In this case it was determined that the signal power level at the system front-end input must be between 13.13 dBm and 16.33 dBm for a successful transmission.

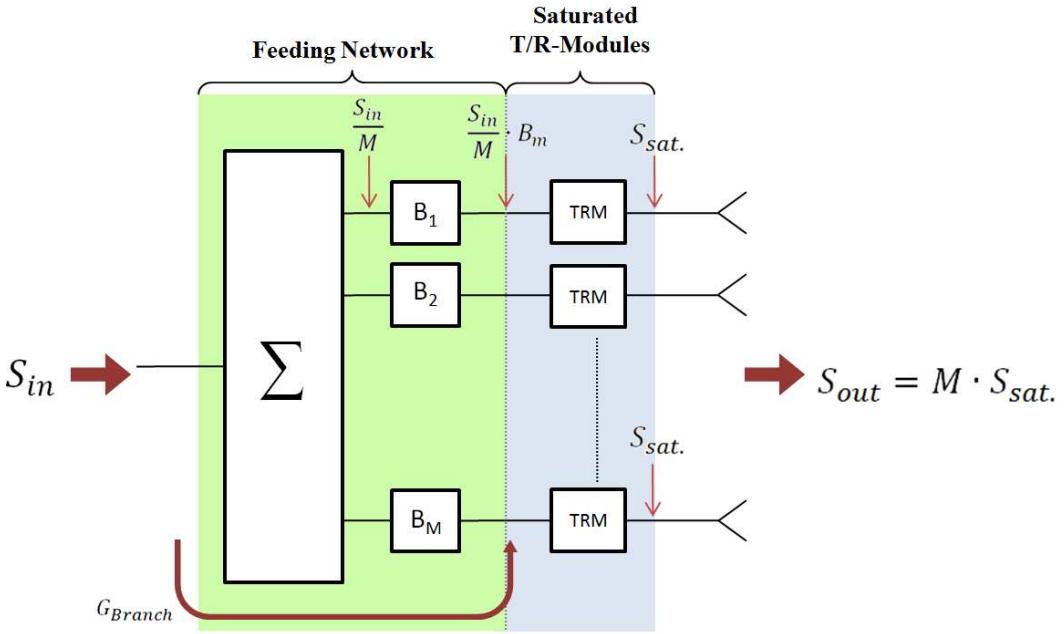


Figure 4.3.1: Schematic representation of the feeding network in transmission mode.

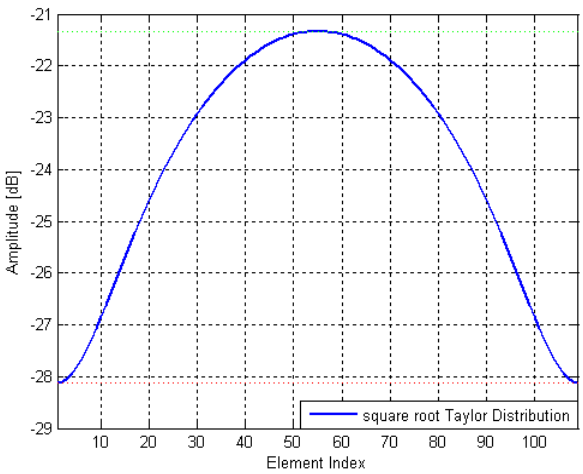


Figure 4.3.2: Taylor tapering applied in transmission mode.

Figure 4.3.3 shows not only the Taylor distribution taper used in reception mode but the square root Taylor distribution present in the feeding network (either transmission or reception mode) as well.

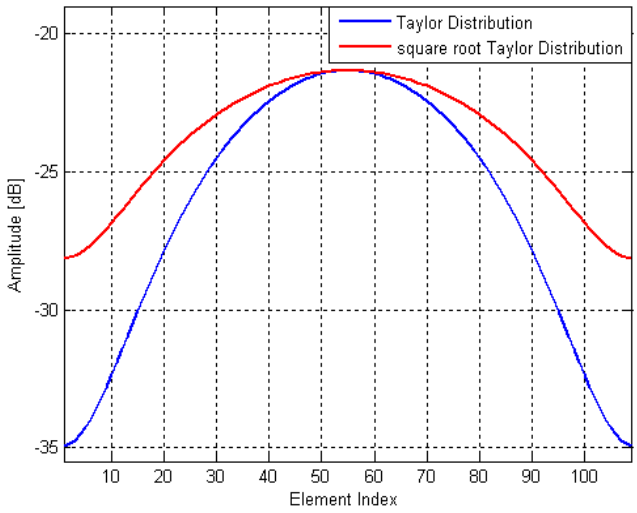


Figure 4.3.3: Confrontation between Taylor and square root Taylor distributions.

As mentioned in Chapter 3 the signal generated by the RF source is going to be used also as the local oscillator input signal needed for the I&Q demodulator in the receiver to achieve the base-band demodulation. In order to have the same signal available for two different inputs a power splitter is required. This component will be placed right after the RF signal generator as shown in Figure 4.4.1. The input LO of the I&Q demodulator, as for every real component, has power restrictions. In this case the I&Q demodulator allows the use of a input LO signal with power level between -6 and +6 dBm.

These restrictions together with the previously found needed power level at the system front-end input, will determine the valid linear dynamic range of the transmitter. The linear dynamic range is the range of signal power levels that can be generated by the RF source that allow the transmitter to work in linearity and at the same time satisfy the power requirements of the system front-end. The procedure to calculate the valid linear dynamic range took into account all the maximum input powers of the components belonging to the transmission path, so none of them will suffer any damage.

Table 4.3.1: Estimation of transmitter gain and valid linear dynamic range.

Estimated Parameter	Value
RF Power [dBm]	-2.68...1.98
Valid Linear dynamic Range [dB]	4.67
Transmitter Gain [dB]*	8.14 ... 16.33

* Assuming that the RF source generates a signal power level equal to 0 dB.

4.4 COTS Based Transmitter

The characteristic of the components shown in this section, as well as those in the section 4.2 corresponds to the actual components that were bought or constructed for the system back-end demonstrator.

Figure 4.4.1 illustrates the final transmitter block diagram adapted to the selected COTS for its construction. Notice that this design has been built based on the assumption that the RF source generates a stable signal with power level in accordance with Table 4.3.1. Actually for the construction of this system back-end prototype the RF source has been set to work at 0 dBm.

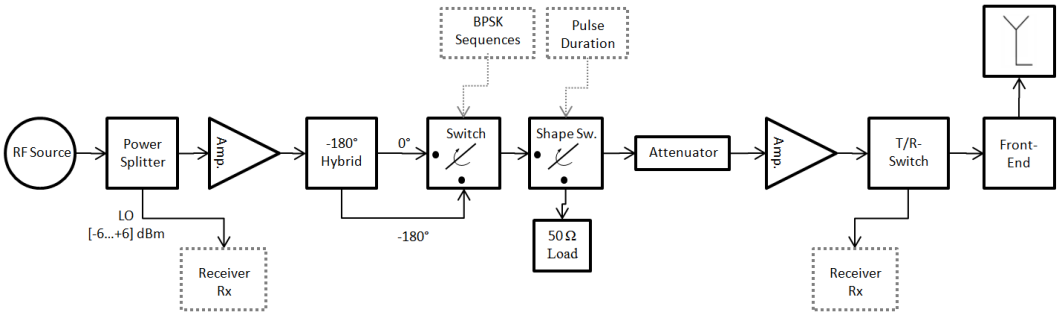


Figure 4.4.1: COTS-based transmitter block diagram.

In the transmitter an attenuator has been added. It is due in order to build a linear system as required, to provide the conditions where all components work in linearity. For this reason the 6 dB attenuator has been included. This component protects the following amplifier not to be saturated

before reaching the necessary signal power level that is required to be delivered to the system front-end.

It is important to remark that the lengths of the cables used to connect the 180° hybrid outputs with the modulation switch inputs are a variable that must be considered as a significant different between these cable lengths will produce a phase different that does not correspond to 180°.

Table 4.4.1 lists the gain characteristics of all the selected components that have been placed in the transmission path. It is important to remark that as has been considered in the receiver case, to assure that the system can be built based on these components the saturation of the individual components has to be taken into account. This consideration allows to predict if any of the components placed in the transmission path could suffer any damage due to power limitations.

Figure 4.4.2 exhibits the results of the power level plan for the transmission path. It shows the curve of signal power level along the transmission path, which is the same for the three operating modes. The level at stage 1 corresponds to the output of the RF signal generator whose signal power, as mentioned above, has been selected equal to 0 dBm. The stage 9 (indicated with a red point) represents the output of the T/R switch in transmission mode, or in other words the system front-end input. In red has been also highlighted the range of signal power levels at the T/R switch output that allow to saturate all the T/R-modules regardless of the attenuation that the feeding network will provoke to the signal. Stage 10 (indicated with a green point) represents the power delivered to the T/R Modules (in the graphic is shown just the value of the center element of the array) due to the tapering. In the same way has been indicated in green lines the input signal power level range of the T/R-modules. The input power of all the T/R-modules must be contained between these limits for the well functioning of the modules and to produce no aperture tapering. If the power condition for the stage 9 (shown in red) is satisfied, the power condition of all the T/R modules will be as well.

Table 4.4.1: Measured gain of the transmission path stages.

Stage	**Component**	**Gain [dB]**
1	RF Source	-
2	Power splitter	-3.32
3	Power Amplifier n°1	15.54
4	Hybrid -180°	-3.29
5	Modulation Switch	-1.15
6	Pulse Shaping Switch	-1.45
7	Attenuator	-6.12
8	Power Amplifier n°2	15.61
9	T/R Switch	-1.5
Total		**14.32**

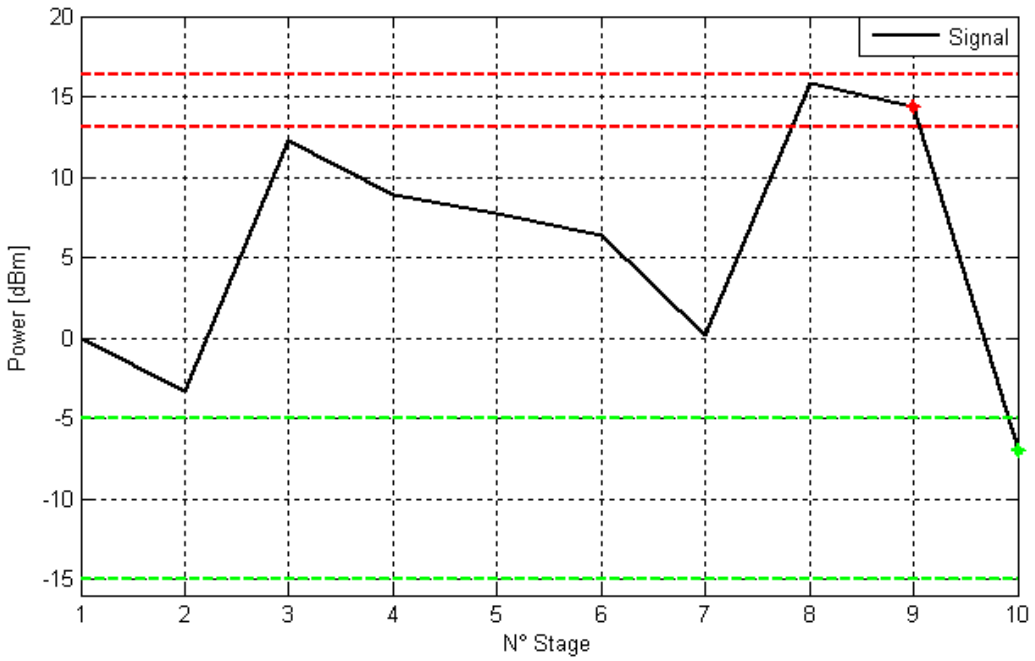


Figure 4.4.2: Signal power level along the transmission path.

Chapter 5

Component Selection for the Transceiver Assembly

In this section all the components used to build the transceiver prototype are presented, exposing their main features and advantages. More information about these devices is provided in annex-A. This annex contains all the datasheets of the used components.

5.1 Main Operational Characteristics

Prior to list all components and their main features, in the following will be briefly recalled the main characteristics that have been taken into account for the selection.

- Gain:

  The gain is the ratio of output to input power or amplitude, and is usually measured in decibels. The gain through a component is constant for a given frequency if this is operating within its linear region. This parameter is one of the most important to considerer for the selection process. The sum (in dB) of all the component gains in the receiver path and the transmitter path must at least be equal to

the estimated gains (Chapter 4) for the receiver and the transmitter respectively.

- Noise Figure:

  As explained in section 2.3, the noise figure is a measure of the degradation of the signal-to-noise ratio, caused by components in the RF signal path, for a specific bandwidth. This parameter is of vital importance for the receiver design due to the fact that the noise power level has to be controlled to obtain the desired signal-to-noise ratio at the receiver.

- Maximum Input power:

  This parameter represents the absolute maximum values of signal power level that a dispositive or component can handle at its input without suffering any damage.

- 1 dB Compression or Saturation point:

  As the input signal is increased in power, a point is reached where the power of the signal at the output is not amplified by the same amount as the weaker signal. The 1 dB compression point has been reached when the input signal is amplified by an amount 1 dB less than the linear signal gain. This parameter is characteristic for many devices as amplifiers, diodes, mixers, etc.

- Maximum output power:

  A rapid decrease in gain will be experienced after the 1 dB compression point is reached. For this reason it is important to take into account the maximum power that a component can deliver at its output if it is working in saturation, especially if it is followed by other devices.

- Insertion Losses:

  They represent the signal power losses due the insertion of a dispositive in the signal path. This is a measure of attenuation and can be consider as a decrease of the component gain.

It is important to remark that all the gain and noise figure values shown in this chapter generally do not exactly agree with the typical values listed in the respective datasheets of the components. This is due to the fact

that gain and noise figure measurements were performed for each individual dispositive in order to have the most realistic value at 3GHz for the PLP analysis.

5.2 Receiver COTS

5.2.i Low Noise Amplifier (LNA)

The LNAs used to build the receiver are of the surface mount monolithic amplifier Gali-39+ which is manufactured by Mini-Circuits. These are wideband amplifiers that offer a high dynamic range and are internally matched to 50Ω. The main applications in which this device is typically used includes communication receiver and transmitter constructions. As this is a surface mounted device, the evaluation board TB-409-39+ was ordered which includes DC blocks for all the inputs and output, and makes use of SMA connectors. The main characteristics of one of the used evaluation board at 3GHz are listed in Table 5.2.i.1.

Table 5.2.i.1: TB-409-39+ electrical specifications.

Parameter	**Value**	**Units**
Frequency Range	DC-7	GHz
Supply Voltage	±12	V
Max. Operating Current	55	mA
Gain @3GHz	17.71	dB
Noise Figure @3GHz	3.13	dB
Max. Input Power	13	dBm
Input 1dB Compression Point	-4.6	dBm
Max. Output Power	13.87	dBm
Input Return Loss @3GHz	-13.71	dB
Output Return Loss @3GHz	-29.36	dB

The Gali-39+ amplifiers have been chosen for this application first of all due to their high gain and low noise figure. Eq. (4.2.1) demonstrates how the noise figure of the total system ends up being approximately equal to the noise figure of the first stage if the gain of this component is high enough to reduce the effect of the subsequent stages. On the other hand, this amplifier provides a large dynamic range as its input 1dB compression point is at a considerably high level with respect to the signal power level expected to receive.

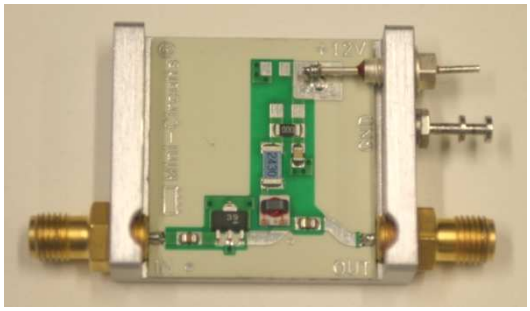


Figure 5.2.i.1: Photograph of TB-409-39+.

5.2.ii Limiter

The purpose of including a limiter before each LNA, is to protect the amplifier of exceeding its maximum input power level. For the receiver construction were selected the broadband limiter RLM-33+ manufactured by Mini-Circuits. These are surface mounted packaged devices that protect against electrostatic discharge (ESD) and input power higher than 12 dBm that surges over its frequency range. These limiters have been used to provide excellent protection of low noise amplifier in communication system applications. For the construction of the receiver prototype the evaluation board TB-393 has been ordered.

Figure 5.2.ii.1 shows the behavior at 3GHz of the signal power level at the TB-393 output with respect to the signal power level at its input. Notice that the output of the evaluation board never exceeds a level of 9.5 dBm. Therefore, the LNA will always be protected as the limiter will not allow the signal power level at the LNA's input to exceed this value, and never exceed

13 dBm which is the maximum power level that the LNA can handle without breaking.

Table 5.2.ii.1: TB-393 electrical specifications.

Parameter	Value	Units
Frequency Range	30-3000	MHz
Gain @3GHz	-0.41	dB
Noise Figure @3GHz	0.418	dB
Input 1dB Compression Point	4	dBm
Max. Input Power	2	W
Max. Output Power	9.49	dBm
Input Return Loss @3GHz	-21.81	dB
Output Return Loss @3GHz	-22.07	dB

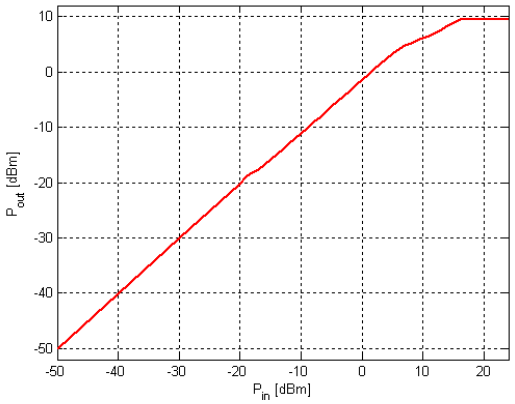


Figure 5.2.ii.1: TB-393 output power vs. input power graph.

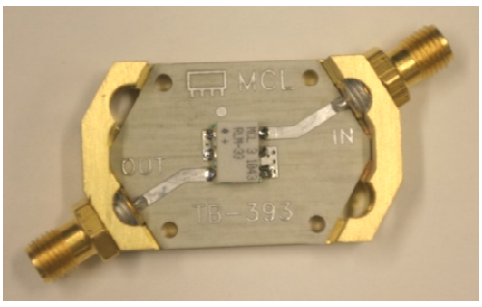


Figure 5.2.ii.2: Photograph of TB-393.

5.2.iii Band-Pass Filter

The ceramic band-pass filter BFCN-3010+ manufactured by Mini-Circuits is one of the few commercial band-pass filters that can be used at 3GHz. It has a good VSWR (1.6:1 typical), small dimensions and good temperature stability. In order to use it for the back-end, it was necessary to order the demo board TB-270 which provides SMA connectors matched to 50Ω.

Table 5.2.iii.1: TB-270 electrical specifications.

Parameter	Value	Units
Frequency Range	2.92-3.1	GHz
Gain @3GHz	-2.347	dB
Noise Figure @3GHz	2.343	dB
Max. Input Power	28.24	dBm
Input Return Loss @3GHz	-22.33	dB
Output Return Loss @3GHz	-17.34	DB

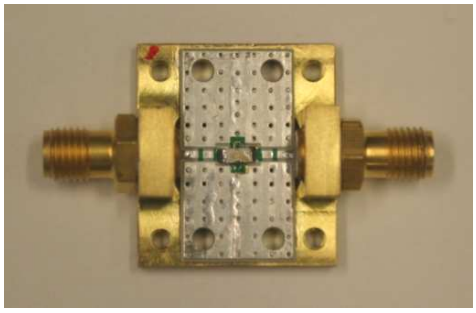


Figure 5.2.iii.1: Photograph of TB-270.

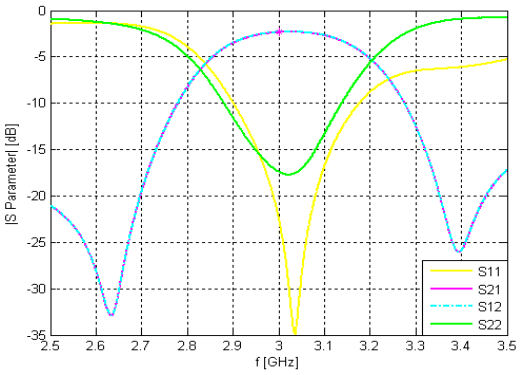


Figure 5.2.iii.2: Scattering parameters plot of TB-270.

5.2.iv I&Q Demodulator

During the search for suitable elements the ADL5380 active broadband I&Q demodulator manufactured by Analog Devices was found. This device

covers an RF/IF input frequency range from 400 MHz to 6 GHz. The ADL5380 demodulator offers remarkable dynamic range suitable for the demanding infrastructure of direct-conversion requirements. The ADL5380 comes with differential RF inputs and baseband output ports which are capable of driving a maximum of 2 V p-p differential signal into differential impedance as low as 200Ω.

Table 5.2.iv.1: ADL5380 electrical specifications.

Parameter	**Value**	**Units**
Frequency Range (RF and LO inputs)	400-6000	MHz
Noise Figure	14	dB
Max. RF Input Power	15	dBm
Max. LO Input Power	13	dBm
Supply Voltage	5.5	V
LO input level	-6...+6	dBm
RF Input 1dB Compression Point	10	dBm
RF Input Return Loss @3GHz	-10	dB
Demodulation Bandwidth	390	MHz

In Table 5.2.iv.1 are shown the electrical specifications of the ADL5380. Notice that the fact that this device has a relatively high noise figure does not really affect the total noise figure of the receiver as the I&Q demodulator has been placed near the end of the reception path, and its noise contribution is reduce by the high gain of the LNAs. Notice as well that the input 1 dB compression point of this demodulator allows a large linear dynamic range.

For the construction of the receiver prototype, evaluation boards of the ADL5380 were ordered. There are two versions of the board, optimized for performance within separate frequency ranges. The internal impedance of the differential baseband ports of both evaluation cards is 450 Ω. For operation below 3 GHz, an FR4 material-based board with the Mini-Circuits TC1-1-13 balun at the RF input is available. On the other hand, for operation between 3 and 6 GHz, a Rogers material-based RO3003 board with the Johanson

Technology 3600BL14M050 balun (optimal for operation between 3 and 4 GHz) at the RF input is available. Both boards can be used for a single-ended or differential baseband analysis. The default configuration of the board is for single-ended baseband analysis. For that configuration the Mini-Circuits TCM9-1 base band balun is provided at the base band output. This balun transforms the 450Ω differential to 50Ω single-ended load. However, the TCM9-1 is realized with a transformer that does not work down to 0 Hz. As 3GHz is the frequency where both cards are supposed to work both evaluation boards were ordered.

Table 5.2.iv.2: ADL5380 evaluation boards.

Evaluation Board	**Frequency Range**
ADL5380-30A-EVALZ	400-3000 MHz (Low Band)
ADL5380-29A-EVALZ	3-4 GHz (Mid Band)

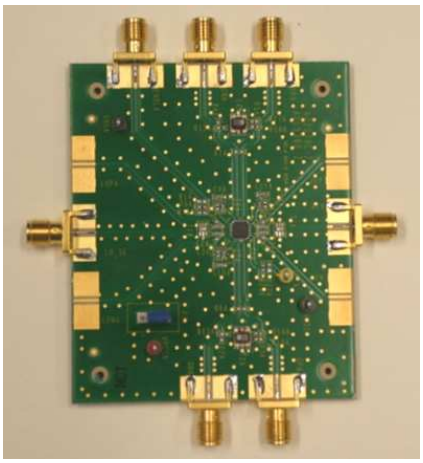


Figure 5.2.iv.1: Photograph of ADL5380-30A-EVALZ.

5.2.v Active Differential Input/Single-ended Output Low Pass Filter

Due to the limited output voltage range of the ADL5380 and the also limited input voltage range of the ADC, the idea of placing commercials low pass filters between the I&Q demodulator outputs and the ADC inputs seemed inadequate and poorly optimized. Inserting commercial low pass filters

besides of adding losses to the reception path, does not allow to control the voltage level of the signal in order to match these two voltages ranges. The evaluation boards used for the ADL5380 have included a balun which reduces the original ADL5380 output voltage range and adds also losses to the path. This balun is supposed to convert the differential (balanced about ground) electrical signal at the ADL5380 output to a single-ended (unbalanced) output signal and to facilitate the connection of lines with 50Ω impedance.

Based on what was stated above, it was decided to design an active differential input/single-ended output low pass filter that substitutes the balun used on the I&Q evaluation board and satisfies at the same time the required low pass filtering. This filter must first of all perform as the balun, presenting a 450Ω load to the ADL5380. Second of all this design must provide at its output a single-ended signal which represents the already filtered in-phase or in-quadrature component of the echo signal.

As the down-converting done by the I&Q demodulator provides the components of the echo signals in baseband, the bandwidths of these are given by half of the bandwidth of the original echo signals bandwidths shown in Table 2.8.1. Considering that the filtering made by this dispositive has to be the same regardless the operating mode in which the radar system is working, it becomes obvious that the -3dB cutoff frequency of the low pass filter must correspond to 5MHz. The reduced bandwidth of the mid and far range mode will be realized by oversampling and digital filtering at the signal processing stage of this radar system.

Table 5.2.v.1: In-Phase and In-Quadrature components bandwidth.

	Close Range	**Mid Range**	**Far Range**
Component Echo Signal Bandwidth B_w [MHz]	5	2.5	1.75

The basic concept of a low pass filter consists in a dispositive that allows all the signal components situated at low frequencies to pass through without any changes, while totally cancelling those components that are

situated at frequencies higher than the cutoff frequency of the filter. This kind of filter unfortunately is impossible to build in practice with a limited number of elements that is why this concept is known as the ideal low pass filter. Filters of first and second order are practical circuits that approximate in an acceptable way the desired ideal response of the filter. However, when it is necessary to filter a signal in a precise way or in order to avoid interferences, the filter needs to behave as similar to the ideal filter as possible, thus filters of higher orders than two (2) are needed [Mal00]. Several approximation functions that are important for filter design have been developed over the years; nevertheless the most known and simplest ones are the approximations of Butterworth and of Chebyshev.

The Butterworth approximation is known for generating the filter of maximum flatness. On the other hand, the Chebyshev approximation generates filters with a certain ripple or gain variation in the pass band that can be controlled by the designer. Allowing for this ripple to occur, the Chebyshev filters provide a higher attenuation of the high frequency components of the input signal than the Butterworth filters [Mal00].

As the low pass filter needed by this system must filter signals with different bandwidths, a flat response of the filter at low frequencies seemed to be the best way to satisfy the requirements of the system, no matter the operating mode under which it is working. For this reason, the Butterworth approximation approach has been selected for the design. For the implementation of the filter was used the configurations of the basic RC active low pass filter and the Sallen-Key low pass filter.

As can be seen in Figure 5.2.v.1 the first stage of the filter consists of a simple RC active low pass filter that has been modified to its differential input configuration in order to satisfy the requirements that have been specified above. As the ADL5380 must be loaded with impedance equal to 450Ω, the two resistors R1 and R2 have been selected in a way that satisfies the condition shown by Eq. (5.2.1) and provide an input impedance of 450Ω as well.

$$Z_{in} = R1 + R2 \tag{5.2.1}$$

The following stages of the filter are Sallen-Key filters that have been designed based on the fifth order Butterworth polynomial. The easiest way to

provide the differential input that is required by the desired low pass filter, consists in the use of the already mentioned RC active low pass filter as the first stage of the final circuit. However, the Butterworth approximation stipulates that the use of this stage is required only in case of an odd order Butterworth filter. The Butterworth approximation approach consists basically in adding one more Sallen-Key filter in cascade when a filter with the consecutive odd order is desired. For this system the fifth order Butterworth low pass filter has been selected as it shows a higher attenuation for the high frequency components with respect to the third order filter, and it demands a simpler construction involving less operational amplifiers than the Butterworth low pass filter of order seven. The final design of the fifth order low pass filter considering just commercial values for all its components is shown in Figure 5.2.v.1. The resistance R13 placed at the output of the filter, together with the input impedance of the ADC, produces a voltage divider matching in this way the output voltage range of the ADL5380 with the input voltage range of the ADC. The frequency response of the filter is shown in Figure 5.2.v.2 where it is possible to see how it provides a flat behavior until 5 MHz and a high attenuation of the high frequency components. Finally Figure 5.2.v.3 shows the behavior of the filter's output voltage with respect to its differential input voltage.

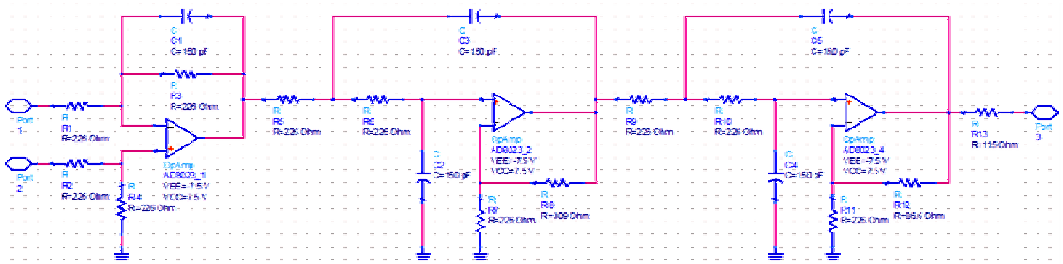


Figure 5.2.v.1: Schematic of designed active differential input/single-ended output low pass filter.

Notice that in Figure 5.2.v.2 the cutoff frequency shows an attenuation of 5.21 dB (with respect with the attenuation in pass-band) instead of an attenuation of 3 dB as is usually done for filters design [Mal00]. As mentioned before, the graphics exposed in this section were obtained using commercial values for all the components involved in the design. For this reason, with

respect to the desired theoretical filter's transfer function, the most similar frequency response that could be obtained from the designed filter was the shown above.

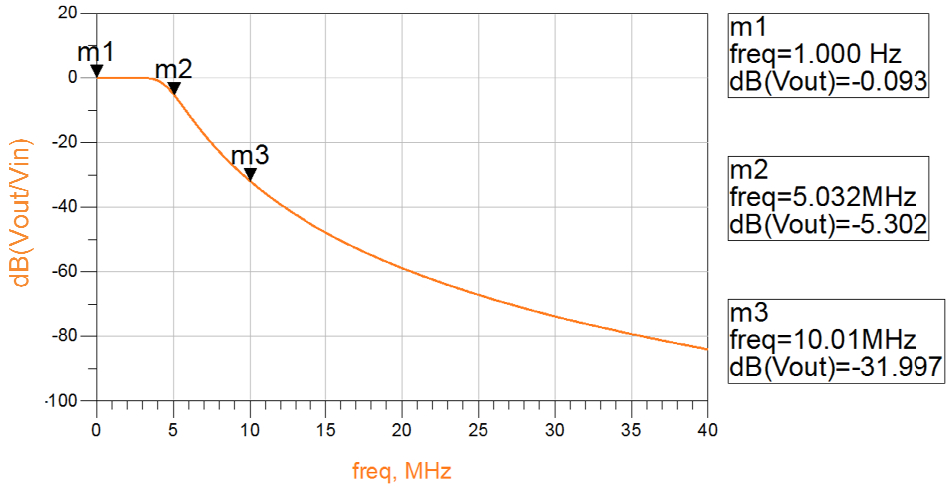


Figure 5.2.v.2: Designed active differential input/single-ended output low pass filter frequency response.

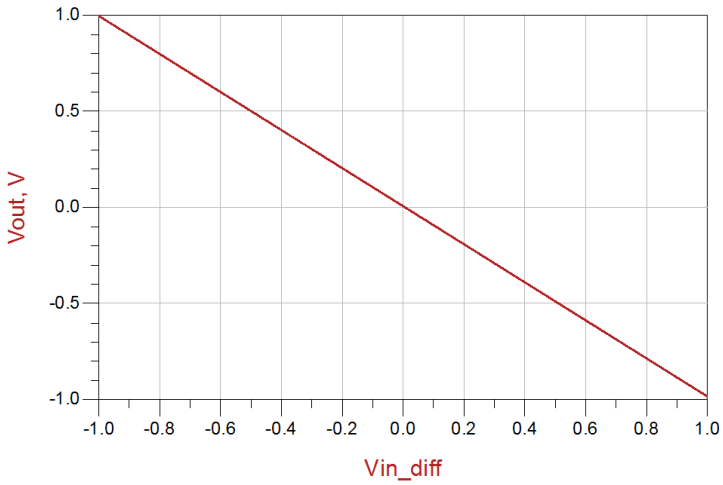


Figure 5.2.v.3: Designed active differential input/single-ended output low pass filter DC response (Vout and Vin_diff are measured in [V]).

For the design and construction of this filter has been selected the operational amplifier AD8023 from Analog Devices. This device is a current

feedback amplifier and features a gain flatness of 0.1 dB to 10 MHz while offering differential gain and phase error of 0.06% and 0.02°. It is important to remark that the design and simulation (including Figure 5.2.v.2) of the filter were done using the Advance Design System (ADS) and the simulation model of the operational amplifier was provided by Analog Devices on their official site.

Before we proceed with the construction of this filter, the analysis of its ideal temporal response is investigated to determine if this filter represents a good approximation of the ideal low pass filter. Using the MatLab language as computing tool, the transfer function in frequency of the designed fifth order filter given by ADS was processed to obtain the temporal response of the filter through the Inverse Fast Fourier Transform (IFFT). With the obtained temporal response, it is possible to estimate how the signal pulses will be theoretically deformed in time by the designed low pass filter. The change of the pulse shape at the filter output is important to consider as the amplitude of the pulse could be reduced, producing some additional losses. The comparison between the ideal 5 MHz low pass filter and the one designed was necessary in order to evaluate the amplitude error that the filter is generating.

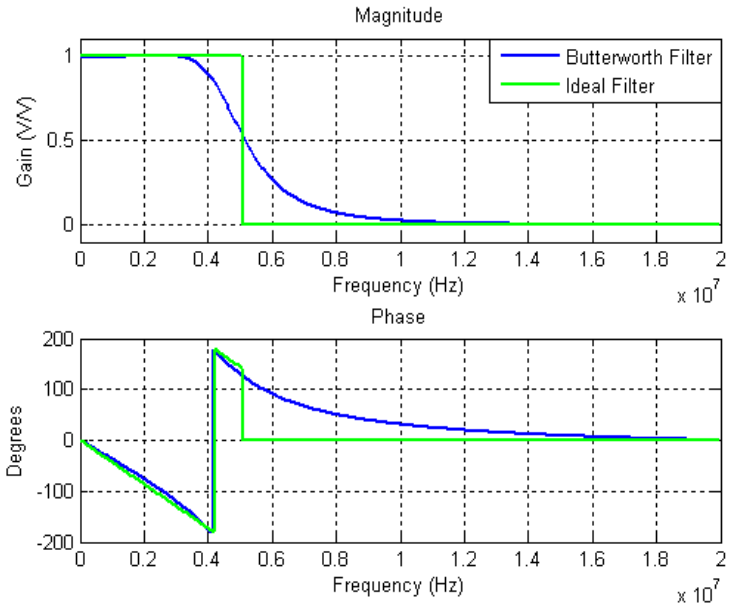


Figure 5.2.v.4: Comparison between the transfer functions (magnitude and phase) of the ideal and fifth order Butterworth low pass filters.

Figure 5.2.v.4 shows the transfer functions (magnitude and phase) in frequency of both ideal and designed low pass filter. The phase response of the ideal filter has been selected in order to force that at its output the signal will show the same time delay that is produced by the designed filter. Figure 5.2.v.5 illustrates the output signals (in time and frequency) of these filters when the input signal is represented by a rectangular pulse of 100 ns (corresponding to the close range mode pulse shape). This pulse shape was selected for the analysis as it constitutes the shortest pulse, thus the worst case. Notice in Figure 5.2.v.4 that the phase of the designed 5th order low pass filter approximates the phase of the ideal filter until the cutoff frequency. The phase of the signal components attenuated by the designed filter is not important.

Observing Figure 5.2.v.5, 120 ns theoretical time delay of the designed filter response can be noted. As mentioned before, the ideal filter does not involve any time delay at its output. For this reason, the phase response of the ideal filter has been chosen so both filters' outputs will show the same time delay and a comparison of their amplitudes can be easily made. The average difference between the ideal and designed Butterworth filter signal output amplitudes for the duration of the input rectangular pulse is about 0.016 V. These characteristics, together with all the results previously shown, make possible to confirm that the 5th order Butterworth filter introduced in this section constitutes a reasonable approximation of the ideal 5 MHz low pass filter.

The next step for the filter design consists in the construction and measurement of its electrical characteristics. Due to the delay in the arrival of the components ordered for the filter construction, it was impossible to build and test the filter on time, so all the important and practical data about it could have been included in this thesis. However, this has to be considered as future work for the system back-end. Regarding this thesis, the main theoretical features of the designed filter are shown in Table 5.2.v.2.

Notice that the gain of the I&Q demodulator and the low pass filter have not been reported due to the change of the analysis form signal power level to the signal voltage level mentioned in Chapter 4. As the filter has been designed to satisfy the voltage characteristics of the I&Q demodulator output and the ADC input, a linear behavior from the demodulator and the low pass

filter have been assumed. The important parameter to examine here is not the input power level anymore, it is the signal-to-noise ratio presented at the ADC input that must be the same that the one at the I&Q demodulator input. The signal and noise power level at the I&Q demodulator input have been characterized to satisfy the SNR requirements of the radar system. However, depending of the configuration of the filter, the signal and noise power levels at the ADC input could be different, but their ratio should be the same. It is significant to remark that in this particular case the design of the active differential input/single-ended output low pass filter has been done in a way that the maximum input signal power of the ADC corresponds to the maximum linear input signal power at the I&Q demodulator, but this characteristic is not mandatory. In general it is enough to respect the input power limitations of the ADC board and to maintain the SNR value presented at the I&Q demodulator input.

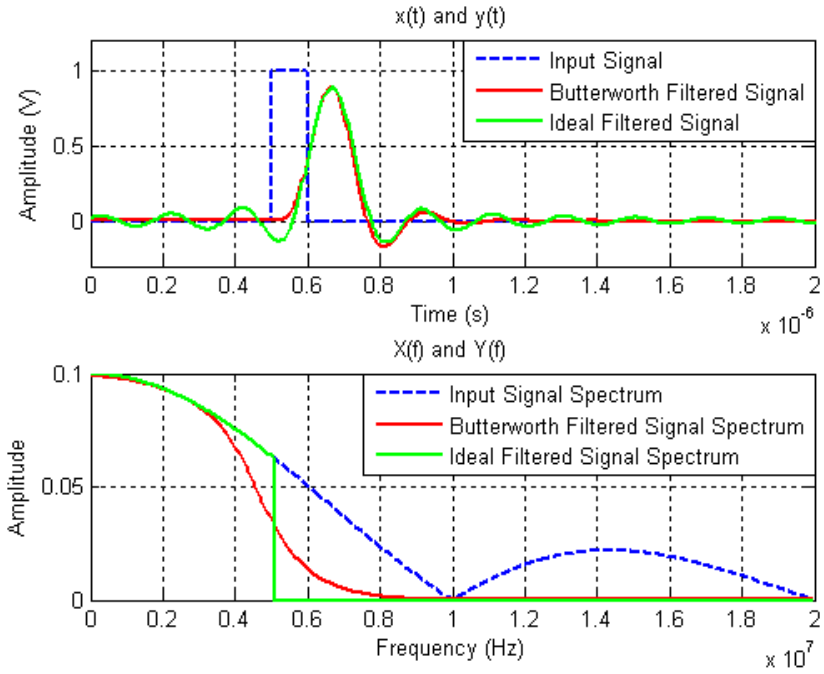


Figure 5.2.v.5: Comparison between the signal outputs (time and frequency) of the ideal and fifth order Butterworth low pass filters for a 100 ns rectangular pulse input signal.

Table 5.2.v.2: Designed active differential input/single-ended output low pass filter theoretical electrical specifications.

Parameter	Value	Units
Frequency Range	DC-5	MHz
Noise Figure (estimated)	10	dB
Max. Differential Input Voltage	±3	V
Max. Output Voltage	1	V
Supply Voltage	±7.5	V
Gain (in pass-band)	-0.093	dB
Input Differential Impedance	450	Ω

5.2.vi Analog-to-Digital Convertor Card

The ADC board is the component in charge for the analog-to-digital conversion of the received echo signals. The ADC card selected to be utilized in the prototype construction of the receiver is the 14-Bit Octopus CompuScope 83XX digitizer manufactured by GaGe. This card is one of the new Gage Octopus™ family of multi-channel digitizers for the PCI Bus. The GaGe digitizer comes with an easy-to-use software development kit for Matlab.

This card was chosen first of all because of its price and its high resolution of 14 bits. However just 11 of these 14 are effective bits. Recall that these values were previously considered for the ADC characterization made in section 4.1. The sampling rate of the board was another important consideration that had to be taken into account for its selection. This model, among several other possible sampling rates, allows to sample the input signal at 10 MSamples/s which corresponds to the sample rate required by this system. The most important characteristic of the 14-Bit Octopus CompuScope 83XX digitizer are listed in Table 5.2.vi.1.

Notice that the on-board memory of the ADC satisfies the requirements of minimum memory needed shown in Table 4.1.1. It is important to consider also that SMA/SMB adaptors are required in order to use this digitizer since all connectors are of the SMB type.

Table 5.2.vi.1: 14-Bit Octopus CompuScope 83XX digitizer characteristics.

Parameter	Value	Units
Number of Input Channels	2	-
Resolution	14	bits
ENOB	11	bits
SNR*	68	dB
Selected Input Voltage Range**	±1	V
Selected Sampling Rate**	10	MS/s
Total On-board Memory	64, 128, 256, 512, 1024	Mbits
Input Impedance (single-ended)	50	Ω

* Measured at 125MS/s in the ±500 mV range with 50Ω input impedance using 10 MHz sine wave with amplitude of 95% of full scale and the on-board filtering capability.

** Correspond to the selected values chosen for this system. More other possible values are presented in the Octopus CompuScope 83XX digitizer datasheet.

Figure 5.2.vi.1: Photograph of Octopus CompuScope 83XX.

5.2.vii Digital Attenuator

The purpose of the digital attenuator stage is to optimize the linear dynamic range of the whole receiver regardless of the operating mode that will be used. The stage "Digital Attenuator" is composed as shown in Figure 5.2.vii.1.

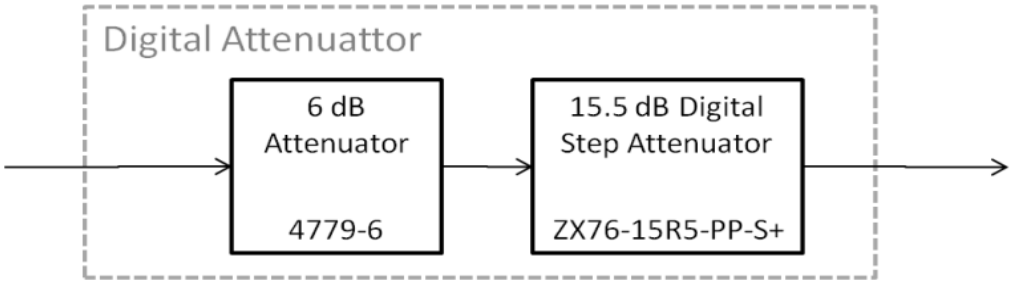


Figure 5.2.vii.1: Schematic of the digital attenuator stage.

This configuration has been chosen due to the digital step attenuator limited attenuation range available. The digital step attenuator has a maximum attenuation of 15.5 dB and the maximum attenuation required by the system back-end was around 19 dB. The ZX76-15R5-PP-S+, manufactured by Mini-Circuits, is a 50Ω RF digital step attenuator that offers an attenuation range up to 15.5 dB in 0.5 dB steps and has a minimum attenuation of 3 dB at 3 GHz. The control is a 5-bit parallel interface. This attenuator includes a ZX76-CP+ shielded cable with interface 25 pin D-type connector J4 and software for its control from the computer.

On the other hand, the 6dB attenuator consists in the 4779-6 passive fixed attenuator, manufactured by narda. The combination of the attenuation given by both attenuators allows to provide the right attenuation to the reception path for each of the operating modes. Table 5.2.vii.1 lists the main characteristics of the ZX76-15R5-PP-S+, 4779-6 and the entire digital attenuator stage, while Table 5.2.vii.2 shows the values of gain and noise figure for the digital attenuator stage which are the objects of interest.

Table 5.2.vii.1: ZX76-15R5-PP-S+, 4779-6 and digital attenuator stage characteristics.

Parameter	**ZX76-15R5-PP-S+**	**4779-6**	**Digital Attenuator**	**Units**
Frequency Range	DC-4	DC-18	DC-4	GHz
Max. Input Power	24	33	30.12	dBm
Gain	-3...-17.7	-6.12	-9.01...-23.82	dB
Power supply	3	0	3	V

Table 5.2.vii.2: Measured gain and noise figure of the digital attenuator stage with respect to the operating modes.

Parameter	**Close Range Mode**	**Mid Range Mode**	**Far Range Mode**	**Units**
Gain	-18.3445	-15.6545	-12.7491	dB
Noise Figure	18.364	15.8105	12.768	dB

The ZX76-15R5-PP-S+ requires the use of DC-blocks at its input and its output. However, since in the evaluation boards of the LNAs, placed before and behind this stage, contain already DC-Blocks it is unnecessary to add more of them to the reception path.

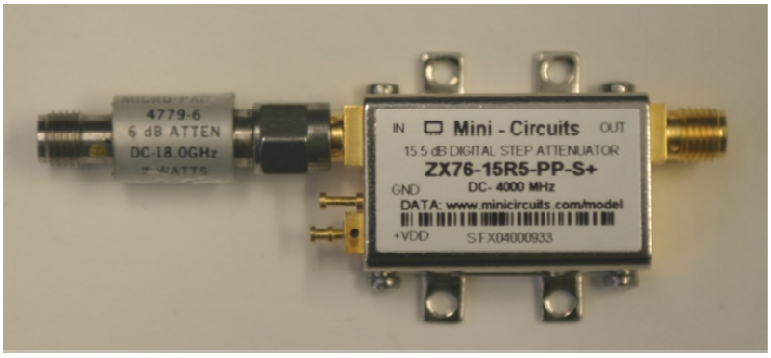


Figure 5.2.vii.2: Photograph of the digital attenuator stage.

5.3 Transmitter COTS

5.3.i RF Amplifier

The RF amplifier selected for the transmitter construction is the surface mount monolithic amplifier GVA-84+ manufactured by Mini-Circuits. This is a wideband amplifier that offers a high dynamic range. The principal applications in which this device has been used includes base station infrastructure, portable wireless, wireless LAN, etc. For the prototype

construction the evaluation board TB-410-84+ was ordered, which includes DC blocks at all RF ports.

Table 5.3.i.1: TB-410-84+ electrical specifications.

Parameter	**Value**	**Units**
Frequency Range	DC-7	GHz
Supply Voltage	±5	V
Max. Operating Current	160	mA
Gain @3GHz	15.54	dB
Max. Input Power	13	dBm
Input 1dB Compression Point	4	dBm
Max. Output Power	20.47	dBm
Input Return Loss @3GHz	-17.81	dB
Output Return Loss @3GHz	-8.04	dB

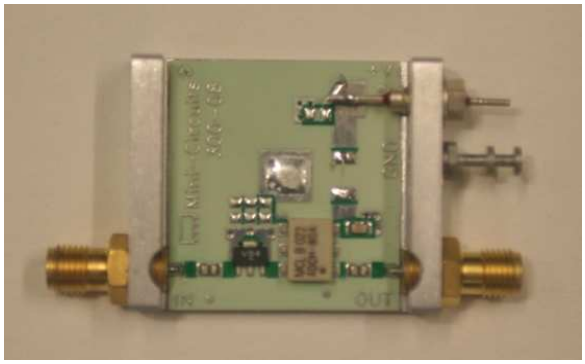


Figure 5.3.i.1: Photograph of TB-410-84+.

5.3.ii Power Splitter

Due to its low price and its low insertion loss value at 3GHz, the 2 way-0°power splitter/combiner ZAPD-4+ from Mini-Circuits has been selected. This power splitter provides a good isolation and can handle high power levels at its input. This dispositive has been use for wireless, instrumentation and communication systems applications.

Table 5.3.ii.1: ZAPD-4+ electrical specifications.

Parameter	Value	Units
Frequency Range	2000-4200	MHz
Gain @3GHz	-3.32	dB
Input Return Loss @3GHz	-18.82	dB
Output Return Loss @3GHz	-22.3511	dB
Reverse Gain @3GHz	-3.32	dB
Max. Input Power	10	W

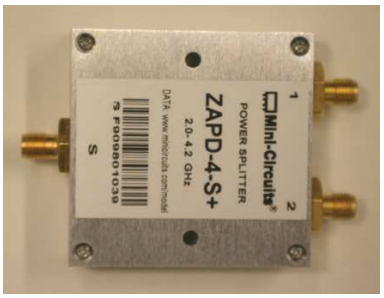


Figure 5.3.ii.1: Photograph of ZAPD-4-S+.

5.3.iii 180 degrees Hybrid

For the prototype construction was selected the 13.00338.01.00 180° hybrid from LYNX. This component features low insertion losses, high isolation, good amplitude, phase accuracy and high power handling.

Table 5.3.iii.1: -180° Hybrid electrical specifications.

Parameter	Value	Units
Frequency Range	2-4	GHz
Gain @3GHz	-3.29	dB
Input Return Loss @3GHz	-18.06	dB
Output Return Loss @3GHz	-16.07	dB
Reverse Gain @3GHz	-3.29	dB
Phase Balance @3GHz	±10	°
Max. Input Power	50	W

Figure 5.3.iii.1: Photograph of 13.00338.01.00.

5.3.iv BPSK Switch (First switch)

This switch is in charge of modulating the 3GHz sinusoidal signal, shifting its phase 180° as is dictated by a fixed sequence. This switch test board has been manufactured Fraunhofer FHR and it utilized the switch SW-475 from MA-COM.

Table 5.3.iv.1: Switch electrical specifications.

Parameter	Value	Units
Frequency Range	0.5-3	GHz
Gain @3GHz	-1.15	dB
Input +1dB Compression Point	27	dBm
Noise Figure @3GHz	1.15	dB
Max. Input Power	33	dBm
Supply Voltage	5	V
Input Return Loss @3GHz	-19.78	dB
Output Return Loss @3GHz	-21.36	dB
Reverse Gain @3GHz	-1.15	dB

Figure 5.3.iv.1: Photography of the test board manufactured by Fraunhofer FHR.

5.3.v Pulse Shaping and T/R Switch

The SW-475 is a low cost SPDT high isolation terminated switch manufactured by MA-COM. These switches protect the T/R modules so they do not have a high RF power always available at the input, just during the pulse time. The pulse shaping switch will turn on and off (depending on the pulse duration and the PRF) the signal that has been generated by the RF source and modulated by the BPSK switch. On the other hand, the T/R switch will change from one input to the other one as it changes from transmission to reception mode and vice versa.

The selection of two different switches is due to the fact that these components where already available in the Fraunhofer FHR's laboratory. However, as the one manufactured by Fraunhofer FHR is just an improvement of the demonstration board made by MA-COM, and the difference in gain between them is 0.3 dB they can be considered as the same switch for what regards this thesis.

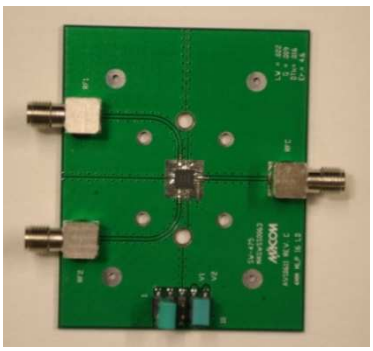


Figure 5.3.v.1: Photograph of SW-475.

Table 5.3.v.1: SW-475 electrical specifications.

Parameter	Value	Units
Frequency Range	0.5-3	GHz
Gain @3GHz	-1.45	dB
Noise Figure @3GHz	1.45	dB
Max. Input Power	33	dBm
Supply Voltage	5	V
Input +1dB Compression Point	27	dBm
Input Return Loss @3GHz	-16.85	dB
Output Return Loss @3GHz	-20.36	dB
Reverse Gain @3GHz	-1.45	dB

5.3.vi Attenuator

The attenuator used here is the same fixed attenuator used inside the digital attenuator stage of the receiver. The 4779-6 passive fixed attenuator, manufactured by narda has been added to the transmission path with the purpose of avoiding that any of the components of the transmitter are operated in saturation when the needed signal power level is being generated. The main electrical specifications are shown in Table 5.2.vii.1.

Figure 5.3.vi.1: Photograph of 4779-6.

Chapter 6

Binary Phased Sequences

The BPSK modulation produced in the transmitter is employed in order to execute pulse compression later on in the receiver. A pulse compression technique has been chosen to compensate the fact that the peak power that can be transmitted by the array antenna is limited. The importance of pulse compression lies on the fact that it allows to transmit more energy by using longer pulses, while increasing the radial resolution by dividing these pulses in shorter sub-pulses. The modulation or coding made in the transmitter could be either a frequency modulation (linear or non-linear) or a phase modulation. However, to be implemented in this system the binary phased modulation type has been chosen.

The transmitter, just in the case of being necessary to detect an object placed within the mid and far range, will modulate in phase the 3GHz signal sub-dividing the long pulses into a specific number of sub-pulses of equal duration; each transmitted with a particular phase. The binary phased sequence then consists of a progression of both +1 and -1 that will be used as the power supply signal of the BPSK switch (see Figure 4.4.1). The switch will choose between the two input signals in accordance with the binary phased sequence selected. As the input signals available correspond to the same signal but with a phase shift of +180° between them, the modulated signal at the switch output will have a phase that alternates between 0° and +180°, generating in this way the sub-pulses.

The matched filter (involved in the pulse compression process) output is described by the phase code aperiodic autocorrelation sequence [CR04]. In order to optimize the system and to guarantee a good performance, it is necessary to know the binary codes with the lowest achievable peak-sidelobe ratio (PSR). The PSR is defined as twenty times the logarithm of the ratio between the amplitude of the higher sidelobe level and the amplitude of the main peak of the autocorrelation function. The presence of high sidelobe levels around and near the main peak of the compressed signal will disturb and confuse the radar [ANB07]. It is for this reason that the selection of the used BPSK sequences is in fact quite critical. In practice it exists a special class of binary codes which are called Barker codes. These codes are also known as optimum because they provide an autocorrelation function with the lowest sidelobe levels possible, which are all of equal magnitude. The autocorrelation function of the Barker codes satisfies the condition that:

$$|R[n]| \leq 1 \qquad \forall\, n \neq 0 \tag{6.1}$$

where $R[n]$ represents the autocorrelation function that will be defined with more detail in section 6.2.

These sequences could also be applied in the complex field if each one of its terms is a complex number with a module equal to one[GS65]. The main problem with these sequences is that just a small number exist. In Table 6.1 are listed all the Barker codes known until this date. Based on the result obtained by [TS61] and recalled by [GS65], it is deduced that no other odd length binary Barker sequence besides those in Table 6.1 exist. On the other hand, the existence of any Barker codes with a even length bigger than four is highly unlikely.

The length limitation of the Barker codes is an obstacle to get better SNR. The relation between the amplitude of the autocorrelation function peak and the sidelobes (PSR) is directly proportional to the sequence length. The sidelobes of the Barker codes have an amplitude of ± 1 as is introduced in [GS65] and [TS61], while the main autocorrelation lobe has amplitude equal to the sequence length. These properties allow the codes to have a more uniform spectrum and better performance in the receiver. Figure 6.1 shows the autocorrelation function for the Barker code of length 13. The PSR is also

proportional to the SNR with which the sequences can be detected by means of the correlation.

Table 6.1: Barker codes.

Length	**Barker Sequence**		**PSR [dB]**
1	+1	-1	0
2	+1 +1	+1 -1	-6.02
3	+1 +1 -1		-9.54
4	+1 +1 +1 -1	+1 +1 -1 +1	-12.04
5	+1 +1 +1 -1 +1		-13.98
7	+1 +1 +1 -1 -1 +1 -1		-16.90
11	+1 +1 +1 -1 -1 -1 +1 -1 -1 +1 -1		-20.83
13	+1 +1 +1 +1 +1 -1 -1 +1 +1 -1 +1 -1 +1		-22.28

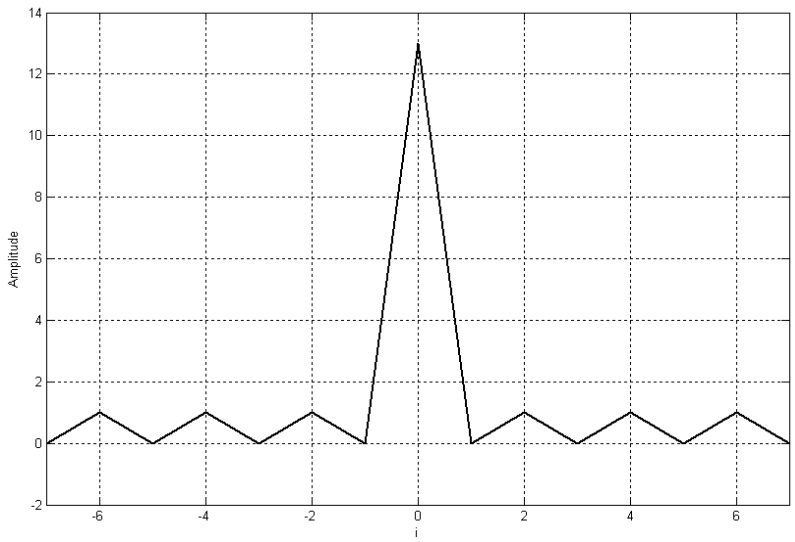


Figure 6.1: Length 13 Barker code autocorrelation function.

In the case of this system, as an SNR of 14.3 dB is required at the output after coherent processing, the binary sequences to be selected must have a PSR maximum equal to -14.3 in order to avoid interference in the signal processing due to the sidelobes amplitude. Taking that into account, all

the Barker codes with length smaller than 7 are considerer useless. The length of the codes or sequences that will be used for the transmitter corresponds to the number of sub-pulses in which is divided the longer pulse when the system operates in mid and far range mode. The lengths of these codes then are shown in Table 2.7.2. Notice that the longest Barker code existing is of length 13 as shown in Table 6.1, so unfortunately it will be impossible to use optimum codes for this system. It is for that reason that in this chapter a thorough search for useful codes that match the system requirements has been done, so the radar will be as much resilient as possible.

6.1 Approaches for the Binary Sequence Search

The existence of unnecessary sidelobes produced by the autocorrelation process yields ghost echoes of targets, which is undesirable for the detection performance of the radar [SS00]. It is for this reason that the main challenge of the pulse compression technique is to minimize the PSL. Since in practical applications, as the radar system under study in this thesis, frequently require sequence lengths longer than 13, a collection of codes with the lowest possible sidelobe level for longer sequences is needed. However up to now there is no accurate solution and effective analytic method to find sequences with the best (lowest possible) sidelobes for the longer lengths. Due to this fact, just exhaustive search methods have been used to generate the best sequences possible. These methods are characterized for being enormously time consuming.

Executing a "full search", which means carrying out a sidelobe level analysis of all the sequences of a determinate length, Linder [Lin75], in 1975, found all the best binary codes up to a length 40 taking for this task about 50 days of work. Years later, in 1990, Cohen *et al.* improving the algorithm extended the result up to length 49 [CFB90]. Afterward using PSL preservers Mertens [Mer96] and consequently Coxson *et al.* expanded the result reaching a length equal to 60 [CR04]. The fact that the computational costs quickly became prohibitive since the cost roughly doubles with each unit increase in code length, provoked the necessity to add new effective optimizations to the

search algorithm, looking now for good rather than the best aperiodic autocorrelation function properties.

In 1967, Boehmer [Boh67] developed an analytical technique for finding good pulse compression codes for any prime code length under 150. Using a Neural network approach, Hu *et al.* [HFD97] obtained useful binary sequences for lengths up to 100. Deng *et al.* [DF99] obtained suboptimum binary sequences with better aperiodic properties than the found with the neural network approach by using evolutionary algorithm (EAs). However the best results registered up to now were obtained by Wang [Wan08], who used an iterated variable depth search (IVDS) algorithm to search for the least autocorrelation binary sequence for a given length. Notice that even with these different approaches, the maximum code length that can be analyzed within a reasonable computation time is up to 100 units.

Due to the large variation of magnitude between the two code lengths that the system requires, different approaches have been taken for each case. For the mid range binary sequences an algorithm of exhaustive search is used as the code length needed is equal to 32 and it is possible to find all the optimum codes in a reasonable computational time. However as the far range binary sequence required has a length of 80, a different algorithm to search for the near optimum binary phased codes is developed.

6.2 Length 32 Codes Search Algorithm Guideline and Results

Recalling that the binary phased sequences consist of a progression of both +1 and -1, the autocorrelation function of an aperiodic N-bit sequence a_n is given by:

$$R(n) = \sum_{i=0}^{N-|n|-1} a_i a_{i+|n|} \quad , \quad n = 0, \pm 1, \dots, \pm(N-1) \tag{6.2.1}$$

And its properties are:

$$R(0) = N \tag{6.2.2}$$

$$R(n) = R(-n) \tag{6.2.3}$$

$$R(n) \leq R(0) \quad , \quad \forall n \tag{6.2.4}$$

$$R(n) = 0 \quad , \quad |n| \geq N \tag{6.2.5}$$

The peak-sidelobe level can be calculated as it follows

$$PSL = \max_{n \neq 0} |R(n)| \tag{6.2.6}$$

The peak-sidelobe ratio (PSR) on the other hand represents the ratio between the PSL and the main lobe of the autocorrelation function.

$$PSR = \frac{\max_{n \neq 0} |R(n)|}{R(0)} \tag{6.2.7}$$

This value is often given in dB, which is obtain calculating the $20 \log_{10}(PSR)$.

The search space of codes, on the other hand, is composed by all the different codes of a specific length N and its dimension is given by:

$$SF = 2^N \tag{6.2.8}$$

As mentioned before a length of 32 bits generates a search space of codes where it is possible to find all the optimum codes by means of an exhaustive search. Therefore the goal of the algorithm in this section is to find all the codes of 32 units that have the minimum PSL and consequently the minimum PSR possible.

The first measure taken during the development of the search algorithm was to reduce the search field, so the computational time will be reduce as well. Based on the autocorrelation properties of the general binary phased codes, the search field can be reduced by the use of the PSL preserves concept.

The PSL preserver refers to the operation that is applied on a binary code a_n that does not produce any change in the autocorrelation or its absolute value. For a known code length N, the use of the PSL preserves provoke a partition of the total search space SF [ANB07]. The PSL preserves used in the design of the algorithm were:

$$b_n = -a_n \quad , \quad 0 < n \leq (N-1) \tag{6.2.9}$$

$$c_n = (-1)^n \cdot a_n \quad , \quad 0 < n \leq (N-1) \tag{6.2.10}$$

as they satisfy the previous established condition that the autocorrelation value must be maintained.

$$|R_a(n)| = |R_b(n)| = |R_c(n)| \tag{6.2.11}$$

Now, thanks to the consideration of Eq. (6.2.9) and Eq. (6.2.10), the entire set of codes can be represented by a subset of one-fourth the size, containing a single code from each equivalent class. The dimension of the new search space is then given by:

$$SF_{eq} = 2^{N-N_{PSL}} \tag{6.2.12}$$

where N_{PSL} is the number of PSL preserver used to reduce the search field.

Finally it was implemented an algorithm that calculates the maximum sidelobe level of all the codes contained in the subspace defined by the use of the PSL preservers. This algorithm selects and saves those codes that exhibit the minimum PSL possible, providing at the end of its operation the compilation of optimum codes of length 32. For the creation of the routine was used the general-purpose, procedural, imperative language of programming known as Fortran. The results obtained with the used of this algorithm are shown in Table 6.2.1.

Table 6.2.1: Full search algorithm results for 32 length sequences.

Code Length	**Total Number of Optimum Codes**	**PSL**	**PSR [dB]**	**Computational Time**	
				Debug Mode	**Release Mode**
32	844	3	-20.56	2h 19m 12s	1h 8m 51.72s

Figure 6.2.1 shows the aperiodic autocorrelation function of one of the optimum 32 length sequences (Table 6.2.2) found with the developed algorithm.

Table 6.2.2: Example of optimum 32 length codes.

Optimum Code	-1 -1 +1 +1 +1 +1 +1 +1 +1 -1 +1 -1 +1 +1 -1 -1 +1 -1 +1 -1 -1 -1 +1 +1 -1 +1 -1 -1 -1 +1 +1 -1

To finalize it should be noted how the codes found in this section satisfy the system requirements due to the fact that the PSR is much lower than -14.3 dB.

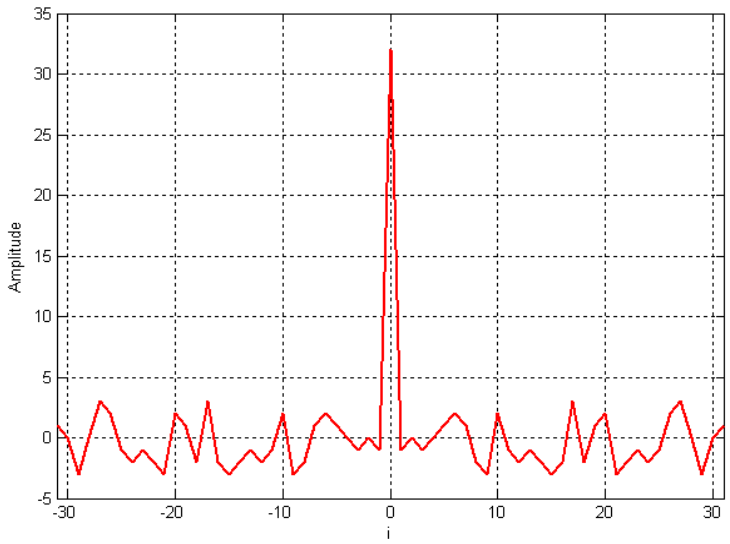


Figure 6.2.1: Example of length 32 optimum code autocorrelation function.

6.3 Length 80 Codes Search Algorithm Guideline and Results

For sequences longer than a 60 units length, as mentioned before, it has not been possible to carry out a search for theirs optimum codes due to the extremely long computational time required. As a 80 units binary phased

code is needed for the system to achieve detection in the far range, a new search method must be apply in order to tackle this problem. The algorithm introduced in this section instead of looking for all the optimum codes of a specific length, it selects those codes that exhibit a PSL reasonably low. This method was inspired by the approach proposed by Deng *et al.* due to the remarkable results shown in [DF99] and the simplicity of the concept which allows to generate results within a small computational time.

Hu *et al.* [HFD97] with a neural network approach found a minimum PSL equal to 8 for sequences of 80 units. Deng *et al.* [DF99] a couple of years later, was capable to find length 80 sequences with a minimum PSL of 6, improving in this way the previous results obtained by Hu *et al.* As the concept of using an evolutionary algorithm to find good codes proved that it is capable of better results than using a neural network approach, a secondary goal of this algorithm besides finding near optimum codes to be used afterwards by the radar system, is to find a minimum PSL that is, at least, equal to the one found by Hu *et al.* in [HFD97]. Therefore, the algorithm must give at the end of its operation a compilation of good codes of 80 units that have the minimum PSL and consequently the minimum PSR found.

The evolutionary algorithm (EA) approach has been inspired by the theory of biological evolution, using for its development the concepts of reproduction, mutation, recombination, and selection. The basic idea behind the EA technique is: given a population of individuals, the environment pressure causes natural selection (selection of the fittest) and this causes a raise in the fitness of the population [ES03]. For the measure of the population fitness it is necessary to establish a quality function to be maximized. Based on the fitness measure of the entire population, some of the better candidates are chosen to seed the next generation by applying recombination and/or mutation to them. The term recombination refers to the action of applying an operator to two or more selected candidates (known as parents), provoking in this way the generation of one or more new candidates (called children). Mutation, in contradistinction to the recombination is applied just to one candidate, producing a new child for each parent. This process can be iterated until a previously set computational limit is reached or it is generated a new candidate that equals or upgrades a certain quality condition.

For the application of the developed evolutionary algorithm the total population corresponds to the 2^{80} binary phased sequences of 80 units in existence. In our particular case, the "fitness" of the population corresponds to the sidelobe level of the individual codes. This will be measured using as quality function the value of PSR which must be minimized in order to get better codes. Trying to keep the evolutionary concept quite simple, the algorithm created does not make use of recombination, applying mutations to a specific group of codes (parents) selected from the total population.

As the parent codes must be composed by several candidates with a high fitness level, a particular group of codes has been selected. Using the algorithm implemented to find the optimum 32 length codes, the codes of 4 and 20 units were found. Taking each one of the found 20 length optimum codes as modulating signals, it has been applied an AM modulation process over the Barker 4 length codes, producing in this way sequences of 80 units. The modulation procedure done to get one of the 80 length codes is shown in Figure 6.3.1. This way there were obtained a total of 12 binary sequences with 80 units, which exhibit a PSL between 19 and 21.

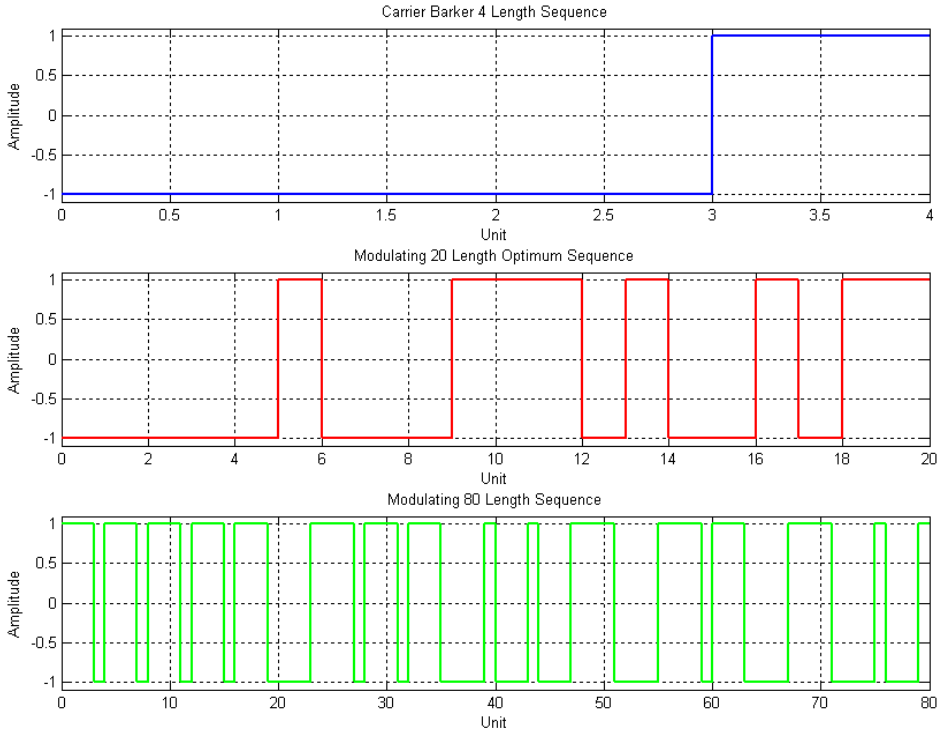


Figure 6.3.1: AM modulation process for the generation of the parents sequences.

These 12 sequences compose the group of parents codes due to the fact that the highest PSR given by these was about -11.6 dB. Several combination of optimum codes where tried in order to select the fittest modulating and carrier sequences to get 80 length sequences. However, the one introduced above had the best values of PSR which will be the starting point of the evolutionary algorithm to obtain final codes with a lower PSR. Notice that the PSR given by the parents codes is quite close to the minimum condition established by the system of -14.3 dB.

Now to generate the children codes, as mentioned before, mutations will be produce. The mutations will be completely random and could affect one or more units of all the parents codes. As the population is composed by binary phased codes, the mutations consist in a simple sign change in the unit(s) or digit(s) of the parent codes selected randomly.

The implementation of the algorithm is quite simple. A limited number of iterations will be specified with respect to the computation time that is available or desired. Each iteration generates one unique 80 length vector of random values between ± 1. The complete collection of parents codes will be mutated in the same code digit(s). For each parent code mutated an unique child code will be generated. Then, for the complete compilation of the children codes the maximum autocorrelation sidelobe level will be calculated. If one or more of the children codes exhibit an improved fitness (lower maximum autocorrelation sidelobe level) with respect to their respective parent code, these codes will become parents by replacing their own in the parent codes group. In this way the fitness of the entire population of parent codes will improve.

The particular code digit(s) of the parent codes that will suffer a mutation will be selected applying a particular condition to the values that compose the generated random vector. For this algorithm the number of mutations that the group of parent codes will experience per iteration is kept small. The condition used to select the code digit(s) to be mutated established that as the random vector has a many cells as the binary sequences digits, the position(s) where this vector exhibits a value greater than 0.9 will determine the digits that will be mutated in the whole collection of parent codes. For example, if the random vector generated shows random values smaller than

0.9 in all its cells besides cell 4 and 20, all the parents codes will be mutated by changing the sign of their digits number 4 and 20.

The fitness of the children codes will be calculated through the autocorrelation function and the determination of the PSL of all them. If the PSL exhibited by a child code is better (lower) than the one shown by its respective parent, this code will substitute its parent in the compilation of parents codes, allowing its reproduction (mutation) in the next iteration.

The algorithm after finishing the limited number of iterations will provide the compilation of parents codes which does not correspond anymore to the original given at the beginning to the algorithm. As the mutation is done randomly, the algorithm can be executed several time obtaining different PSL results. For this reason a restriction of the minimum PSL desired must be applied. As the purpose of this algorithm is to find the minimum possible PSL of the 80 length codes (to provide robustness for the radar system) and at the same time improve the PSL results obtained by Hu *et al.*, the condition established for the selection of the good codes was a PSL maximum equal to 8. The results achieve with this EA are listed in Table 6.3.1.

Even though that the minimum PSL found with this algorithm did not reach the results shown in [DF99], a PSL equal to 7 is better than the results obtained by Hu *et al.*. One more time, as with the 32 length code case, the PSR values obtained satisfy the system requirement by far, reducing the probability of having signal processing error due to the sidelobe levels.

Table 6.3.1: Evolutionary algorithm results for 80 length sequences.

Found Near Optimum Codes	**PSL**	**PSR [dB]**
343	8	-20
30	7	-21.16

Figure 6.3.2 shows the aperiodic autocorrelation function of one of the near optimum 80 length sequences (Table 6.3.2) found with the developed evolutionary algorithm.

Table 6.3.2: Example of 80 length near optimum codes with PSL equal to 7.

Near Optimum Code	-1 +1 +1 -1 -1 +1 +1 -1 +1 +1 +1 +1 -1 -1 +1 +1 +1 +1 +1 +1 -1 -1 -1 +1 -1 -1 +1 -1 -1 +1 +1 +1 -1 -1 -1 +1 -1 -1 +1 -1 +1 +1 -1 -1 -1 +1 -1 +1 -1 -1 +1 +1 -1 +1 -1 +1 +1 -1 -1 +1 -1 +1 -1 +1 -1 +1 +1 -1 +1 -1 +1 -1 -1 -1 -1 -1 -1 -1

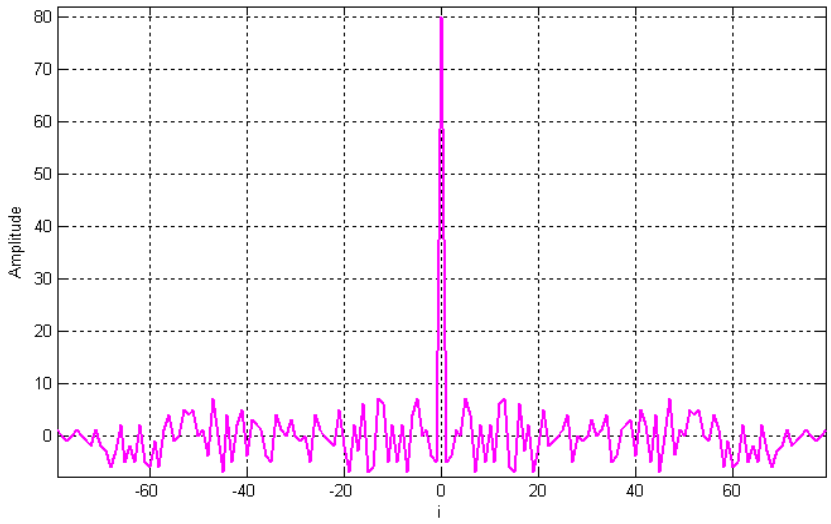


Figure 6.3.2: Example of 80 length near optimum code autocorrelation function.

6.4 Cross Correlation Analysis

First of all let us quickly review the idea of cross-correlation, which is the measure of similarity of two signals, sequences or variables. As the autocorrelation analysis is applied to the sequences obtain in the previous section, the cross-correlation of two codes $a[n]$ and $b[n]$ of the same length N, can be determine as follow:

$$R^{ab}(n) = \sum_{i=0}^{N-|n|-1} a_i b_{i+|n|} \quad , \quad n = 0, \pm 1, \dots, \pm(N-1) \tag{6.4.1}$$

The cross-correlation analysis is quite important for the radar system operation. In order to avoid interference due to objects placed outside the unambiguous range of the operating mode in use, the radar system from one

pulse to the next must change the binary phased sequence used to modulate the pulses. If the radar system maintain the same binary phase code for two (or more) consecutive pulses, the echo signals due to the first pulse coming from targets outside the radar's unambiguous range will be received during the reception time of the next pulse, provoking in this way range ambiguity. For this reason the maximum cross-correlation level between two consecutive sequences must be as low as possible. Notice that the continuous necessity of changing the pulse compression code from one pulse to another was the motivation for finding as many as possible optimum or near optimum codes in the section 6.2 and 6.3.

Other radar systems operation in the same environment represents one source of interference that can confuse the radar system provoking detection mistakes. That is why the sequences are not fixed but must change in a certain way in order to reduce the probability of two coherent radar systems using the same sequence.

The cross-correlation values between the same length codes that have been found are not constant. The analysis employed here consisted in calculating the cross-correlation function between all found codes of the same length, then based on these values the selection of the following codes to use can be done. If one code $a[n]$ presented a high value of cross-correlation with respect to a different code $b[n]$, it indicates that the sequence $b[n]$ does not qualify as a suitable candidate to be used after $a[n]$ during the transmission process. Consequently, if $b[n]$ shows low cross-correlation function values with respect to $a[n]$ that also satisfies the requirements of PSR of the system, the sequence b$[n]$ will be indicated as a candidate, generating in this way for the code $a[n]$ a data base where all its following candidates are accumulated and could be selected from for the modulation of the energy pulse.

For all the best codes found (of 32 and 80 length) were calculated the cross-correlation matrices, which contain the maximum cross-correlation levels between them (for all the possible combinations of code couples with the same length). It is obvious that the diagonal of these matrixes will exhibit the highest values as these correspond to the main peak of the autocorrelation function of each found code.

Figure 6.4.1.a and Figure 6.4.2.a illustrate graphically the cross-correlation matrices for the found 32 length optimum codes and the found 80

length near optimum codes, respectively. As mentioned before, a filtering must be done to these matrices that allow us to determine, for each one of the found codes, those who are suitable to be transmitted consecutively. This filtering is based on the premise that the maximum cross-correlation isolation possible between two codes is desired.

In case of the 32 length optimum codes, the couples of codes with the minimum cross-correlation levels were determined in order to reduce as much as possible the effects mentioned above. The minimum cross-correlation level between 32 length optimum codes is equal to 7, which provides a PSR of -13.20 dB. Unfortunately, just few optimum codes meet this level. Consequently, the trade-off between the number of possible codes and the minimum cross-correlation level for the 32 length optimum codes is critical, as the interference given by the cross-correlation of the codes increases when a larger collection of codes is desired. The minimum cross-correlation level, in this particular case, was raised to 8 (Figure 6.4.1.b) as a significant quantity of codes with this level was available.

For the 80 length near optimum codes, the same analysis was applied. A significant amount of codes were found that have a cross-correlation level equal or smaller than 15, providing a maximum PSR of -14.54 dB. Figure 6.4.2.b shows all the couple of codes that exhibit this cross-correlation level.

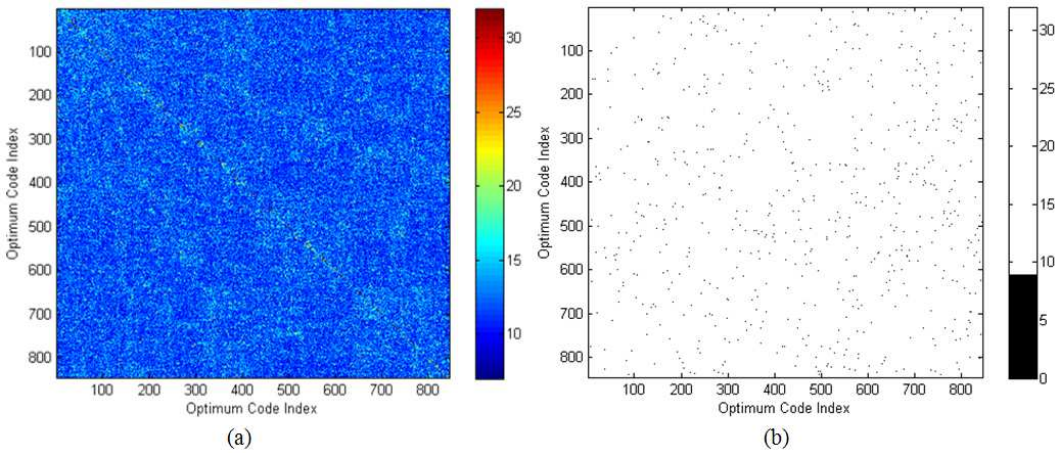


Figure 6.4.1: (a) Graphical representation of the cross-correlation matrix for the 32 length optimum codes. (b) Graphical representation of the cross-correlation matrix for the 32 length optimum codes with a maximum level of 8 (-12.04 dB).

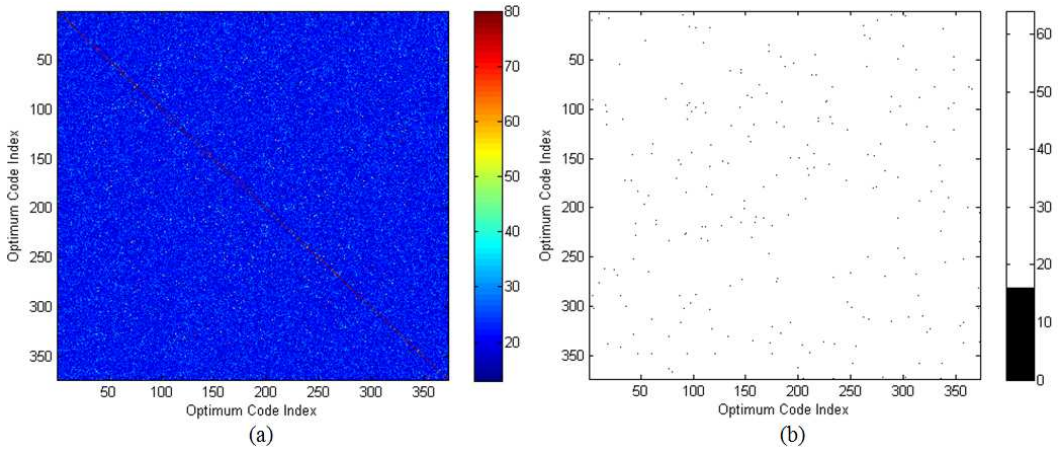


Figure 6.4.2: (a) Graphical representation of the cross-correlation matrix for the 80 length near optimum codes. (b) Graphical representation of the cross-correlation matrix for the 80 length near optimum codes with a maximum level of 15.

Chapter 7

System Back-End Prototype Completion

7.1 Measurement Procedures

In this section will be given a full description of the gain and noise figure measurement procedures. Also will be listed the instruments and component that were used to get all the results shown in the rest of the section.

The gain measurements were done with the help of a PNA series network analyzer E8364B from Agilent Technologies. This instrument measures the scattering parameter of the device under test (DUT) placed between its ports. On the other hand, the noise figure measurement procedure was based on the Y-factor method shown in [ATM]. The ROHDE&SCHWARZ FSU50 spectrum analyzer was used to measure the noise figure of all the components of the system back-end.

Before describing the Y-factor procedure it is necessary to introduce some basic concepts as the Excess Noise Ratio (ENR), noise source and Y-factor itself.

The Y-factor method involves the use of a noise figure source that has a pre-calibrated ENR. The excess noise figure is a temperature-dependent noise ratio. It is defined as the noise that occurs above 290 K which usually corresponds to the room temperature where the measures have being made. Typically ENR is measured in dB and it is calculated with Eq. (7.1.1)

$$ENR = \frac{(T_s^{ON} - T_s^{OFF})}{T_o} \tag{7.1.1}$$

where: T_s^{ON} and T_s^{OFF} are the noise temperatures of the noise source in its ON and OFF states, respectively.

T_o is the reference temperature of 290 K.

For all the noise figure measurements, it was used the NC346V noise source from NOISE COM INC. This has an ENR of 13.73 dB at 3 GHz.

The Y-factor, conceptually, is a ratio of two noise power levels, one measured with the noise source ON and the other with the noise source OFF.

$$Y = \frac{N^{ON}}{N^{OFF}} \tag{7.1.2}$$

N^{ON} and N^{OFF} are measured several times, so that an averaged value of Y can be computed.

The complete Y-factor method requires two steps: calibration and measurement of DUT, as shown in Figure 7.1.1. The first step is done without the DUT in place, connecting the noise source directly to the input instrument. Here a noise reference plane is measured. The second step consists in repeating the Y-factor measurements with the DUT inserted. In this step the spectrum analyzer screen will display the measurements corresponding to the DUTs noise figure.

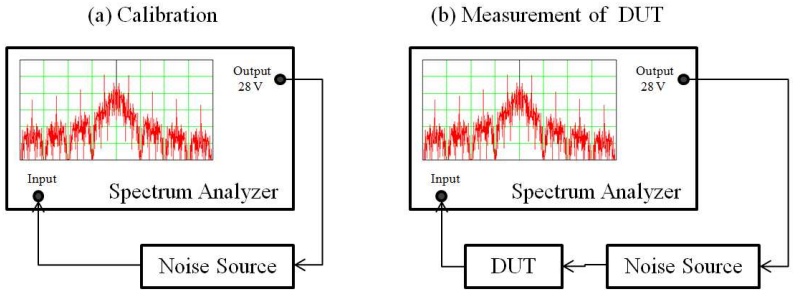


Figure 7.1.1: The Y-factor noise figure measurement.

To know more about the calculations done by the spectrum analyzer in order to determine the noise figure of the DUT, it is recommended to consult [ATM].

As the noise figure instruments are very sensitive, any RF interference either radiated or conducted, will mask as noise power and affect measurement accuracy. During the measurement process, the results obtained, using the Y-factor method as presented above, were quite unstable. For this reason some modifications of the established set-ups for the calibration and for the measurement steps were made. These modifications are shown in Figure 7.1.2 and Figure 7.1.3.

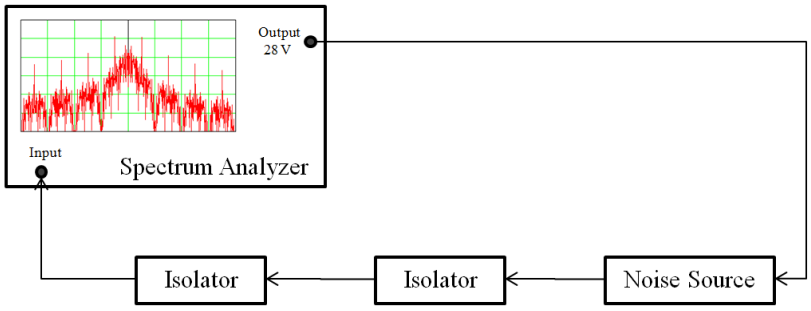


Figure 7.1.2: Schematic of the calibration set-up.

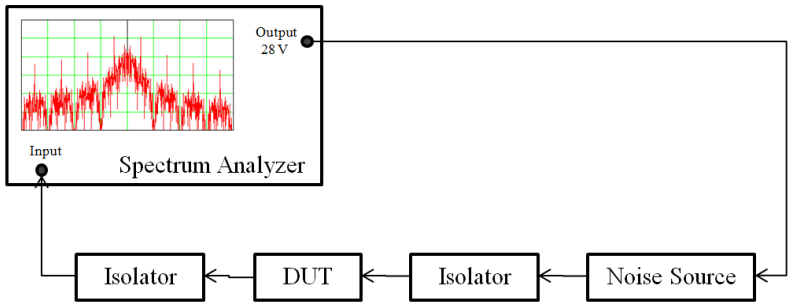


Figure 7.1.3: Schematic of the noise figure measurement set-up.

First of all it is important to remark that, as the noise figures to measure and the ENR given by the noise source are low, the pre-amplifier included in the spectrum analyzer had to be activated to minimize measurement uncertainties. A couple of coaxial isolators were added to the

set-ups with the purpose of improving the matching of the spectrum analyzer, shielding it on its input side from the effects of conditions on its output side. In our particular case, the 200057 isolators by RYT INDUSTRIES were used. This new configuration had showed a significant improvement of the measurement process, allowing to get more stable results of the noise figure measurements.

7.2 Experimental Measurement Results

Most of the gain and noise figure measurement results are shown in chapter 3 and 4, as all the gain and noise figure values of each introduced component, were measured in the laboratory in order to make the power level plan as realistic as possible.

Having all the components for the transmitter and the receiver demonstrator it was necessary to measure the gain and the noise figure of the whole transmission and reception path. As mentioned before, for the transmitter case the noise figure was not measured as the noise power level analysis is not necessary. In order to measure the transmitter and the receiver separately, the T/R switch block was not included in the built set-ups.

For the transmitter, the measurement of the signal gain was made from the power splitter input to the second power amplifier output (stage 2 to 8 of the transmitter power level plan). Figure 7.2.1 shows the transmission path built with all the acquired COTS components. Notice that in order to build the transmitter, it was necessary to add some SMA-M/SMA-M adapters and some cables which added some additional losses with respect to the system shown in Chapter 4. Regarding the cables, these were selected as similar as possible in order to build a symmetrical transmission path, reducing in this way the additional phase difference that they produce between both modulation switch inputs. Due to these new considerations, it was expected in advance a smaller gain than the calculated in Chapter 4. Table 7.2.1 shows the expected value of gain for this transmitter, considering the absence of the T/R-switch and the result of the practical measurement.

Table 7.2.1: Theoretical and measured transmission path gains.

Theoretical expected gain [dB]	**Measured gain [dB]**	**Error [dB]**
15.8197	15.1583	0.66

The error calculated here, as was predicted in advance, can be justified by the presence of several port adapters and cables along the transmission path that were not considered in the power level plan and for the gain estimation. The measured signal gain shown in Table 7.2.1 corresponds to the transmitter path that does not change the input signal phase 180° which will be the signal path in the case of the close range operating mode where no BPSK modulation is applied. For the other two operational modes the transmitter input signal will be divided in sub-pulses that will have a particular phase of the two possible due to the BPSK modulator shown in Figure 7.2.2. For this reason, it was important to measure the gain of both paths and their phase in order to determine how balanced will be the transmitter output signal. These results are listed in Table 7.2.2.

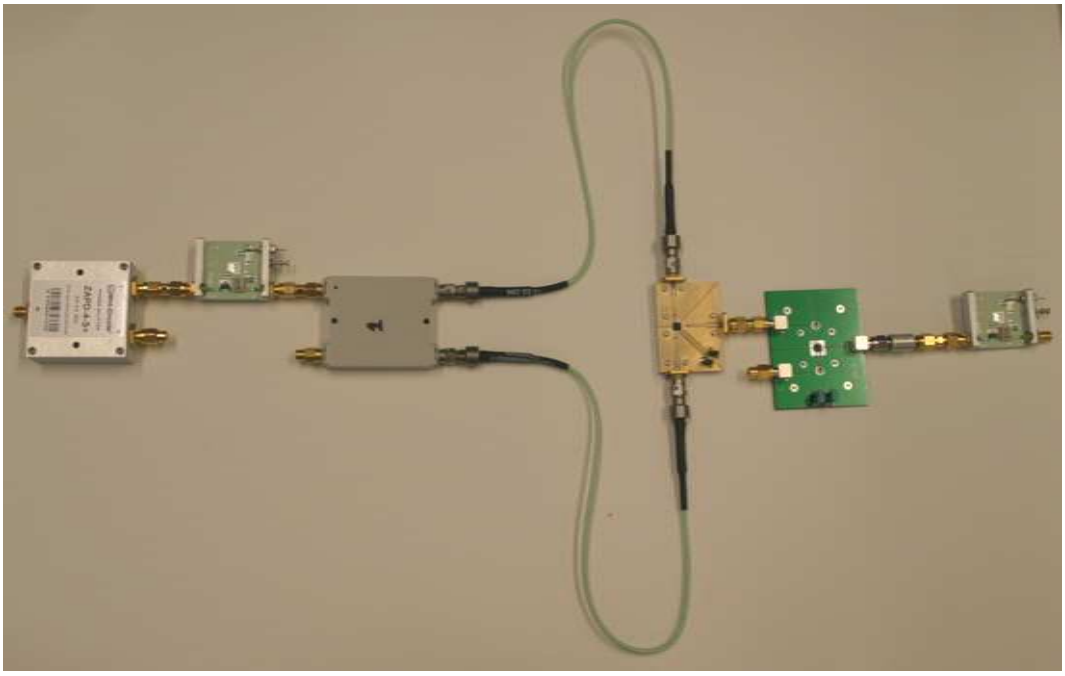


Figure 7.2.1: Photograph of the transmission path built with the selected COTS components.

As the difference between the two transmission paths was less than 0.1 dB in gain (amplitude) and 171.8° in phase, it is possible to confirm that the modulation of the signal was correctly achieved. However, a more precise modulation, where the phase difference between the two signal paths is closer to 180°, can be achieved if the cables involved in the BPSK modulator are manufactured especially to be as similar as possible.

Table 7.2.2: Phase and gain comparison of the two possible transmission signal paths.

Transmission Path	**Measured gain [dB]**	**Measured phase [°]**
0°	15.1583	75.6171
-180°	15.2169	-96.1761
Δ	0.06	171.79

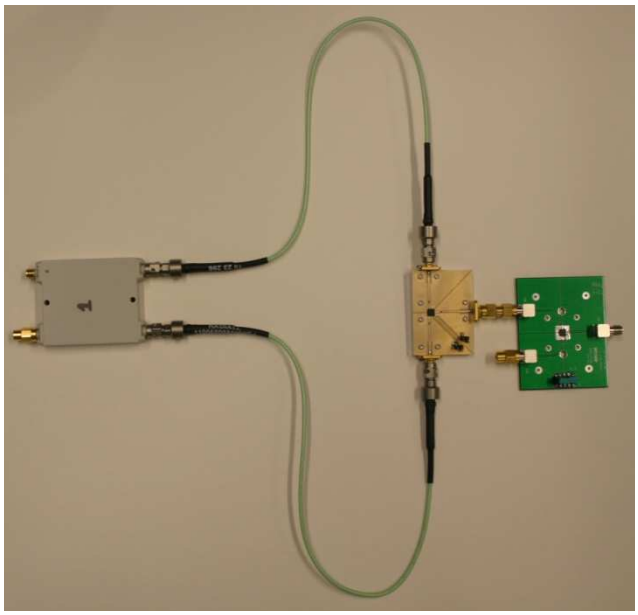


Figure 7.2.2: Photograph of the BPSK modulator built with the selected COTS components.

Finally, the signal gain measured provided by the built transmission path satisfied the power requirements of the system frond-end if this is fed with a RF signal of 0 dBm as has been assumed along this thesis. Under these conditions the transmitter will be able, regardless of the square root Taylor distribution attenuation made by the feeding network, to generate a signal

power level that is enough to saturate all the T/R-modules without breaking any of them.

Figure 7.2.3 shows the scattering parameters of the two signal paths for the built transmitter demonstrator shown in Figure 7.2.1.

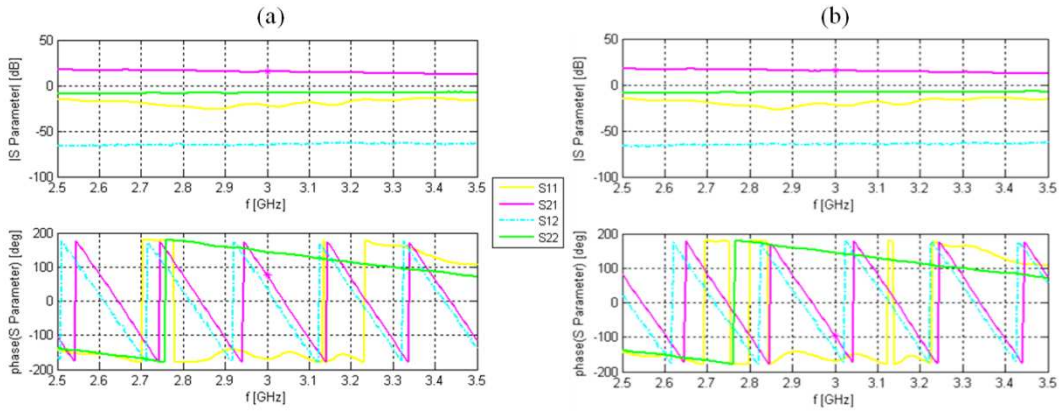


Figure 7.2.3: Magnitude and phase of the S-parameters for the built transmitter demonstrator: (a) 0° signal path, (b) 180° signal path.

With respect to the receiver, the gain and noise figure were measured for the RF part of the receiver which includes all the components from the first LNA (including its respective limiter) to the band pass filter (from stage 5 to 12 of the receiver power level plan). Figure 7.2.4 shows this RF reception path build with all the acquired COTS components. The I&Q demodulator and the designed low pass filter were not considered in the RF receiver path due to the fact that these stages work in base-band and they have been designed to behave linearly, not affecting the gain of the final reception path.

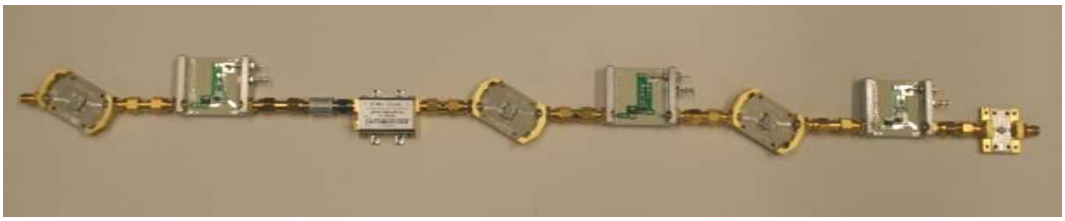


Figure 7.2.4: Photograph of the RF reception path built with the selected COTS components.

In the same way as with the transmitter, the use of SMA-M/SMA-M adaptors was necessary, adding more losses and reducing the signal gain of the receiver path once again. In contrary to the transmitter case, the reduction of the receiver path's signal gain here is quite critical as a minimum signal gain is required. The digital attenuator stage is of vital importance in these circumstances. If due to the losses added for the adapters, the minimum signal gain is not reached, the attenuation given by this stage can be changed in order to fix the situation, trying always to get the largest linear dynamic range possible.

The optimum receiver's signal gain was measured for all the operating modes. The digital attenuator stage value was fixed in order to satisfy the minimum signal gain requirements of the receiver path and providing at the same time the largest linear dynamic range possible with this configuration.

Table 7.2.3: Theoretical and measured minimum signal gain for the RF reception path shown in Figure 7.2.4.

Mode	**Minimum Theoretically Required Gain [dB]**	**Measured gain [dB]**	**Error [dB]**	**Digital Attenuattor Settings [dB]**
A	31.24	31.4812	0.24	3.5
B	33.76	34.0936	0.33	7
C	36.77	36.8996	0.13	9.5

The error calculated here can be interpreted as the part of the theoretical linear dynamic range that could not be used due to the limitations of the receiver prototype. Notice how the use of the digital attenuator stage allows to make the most of the linear dynamic range limited by the ADC.

The plot of the scattering parameters of the RF reception path for all its different configurations is shown in Figure 7.2.5.

Concerning the noise figure, using Eq. (4.2.1) it was possible to calculate the theoretical noise figure expected for the RF part of the receiver path. Table 7.2.4 shows how the noise figure grows while stages are added to the signal path for the different operating modes. In this table are considered

just the components from the stage 5 to stage 12 of the receiver power level plan, which form the RF reception path shown in Figure 7.2.4. Now using the Y-factor method introduced in the previous section, the noise figure for all the different configurations of the reception path was measured. The comparison of the measured and theoretical values of the noise figure is presented in Table 7.2.5.

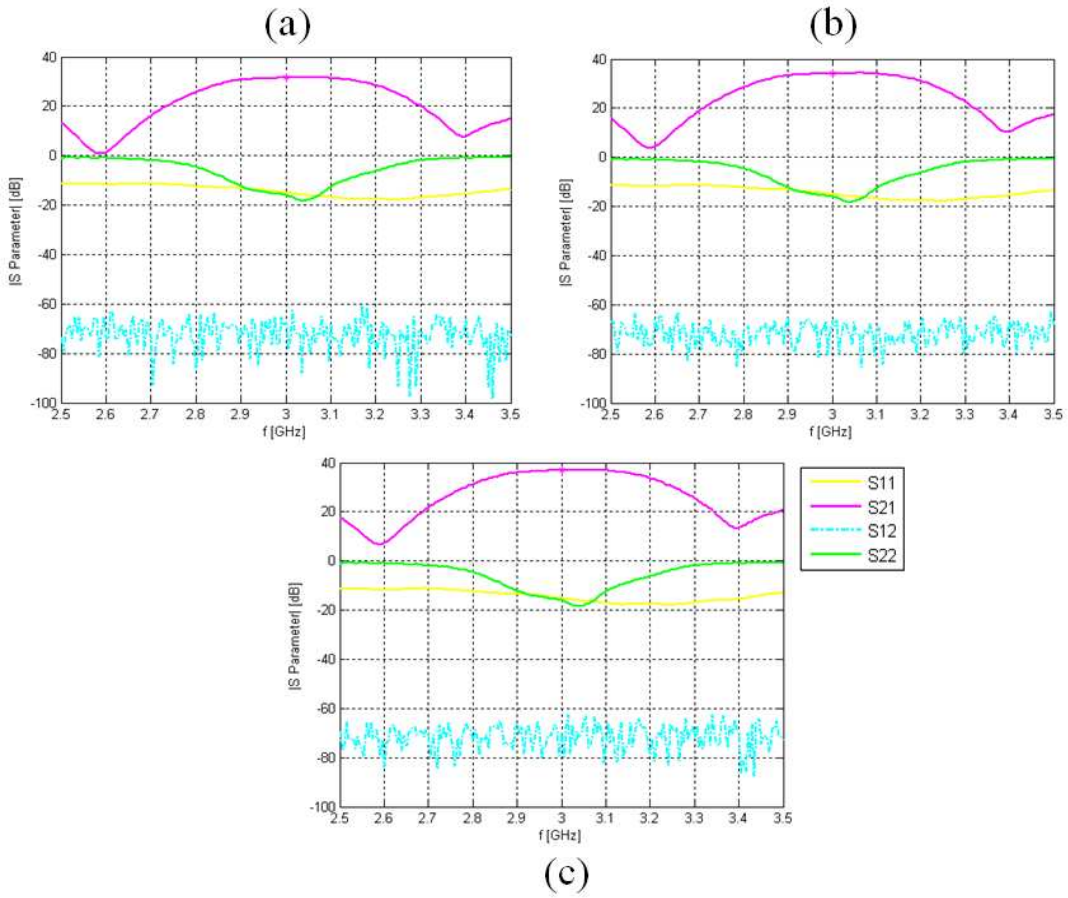


Figure 7.2.5: S-Parameters of the built RF reception path for: (a) close range mode configuration, (b) mid range mode configuration, (c) far range mode configuration.

It can be observed that the measured noise figure is always bigger than the theoretical one. However, as the error between them is quite small the values measured are considered as acceptable. Noticed how in Table 7.2.4 the noise contribution of the last stages does not change considerably the final value of the noise figure. It is for this reason, that it is correct to assume that

no matter how large the I&Q demodulator and the designed low pass filter noise figures are, the final receiver noise figure will remain approximately the same as the one given in Table 7.2.5. The noise figure measured in this partial receiver prototype for most of the cases is larger than the total receiver noise figure equal to 4.8 dB as expected, as has been mentioned in previous chapters. However, it is important to remember that this partial prototype does not include the system front-end and the expected noise figure of 4.8 dB involves the entire reception path. The noise contributions presented here correspond to the system back-end and will be attenuated by the high gain of the feeding network once the reception path is completely built, reaching at the end the expected noise figure value.

Table 7.2.4: Theoretical noise figure along the RF reception path shown in Figure 7.2.4.

		Noise Figure [dB]		
Stage	**Component**	**Close Range Mode**	**Mid Range Mode**	**Far Range Mode**
5	Power Limiter n°1	0.394	0.394	0.394
6	LNA n°1	3.472	3.472	3.472
7	Digital Attenuator	5.380	4.621	4.065
8	Power Limiter n°2	5.525	4.716	4.119
9	LNA n°2	6.957	5.710	4.722
10	Power Limiter n°3	6.959	5.711	4.723
11	LNA n°3	6.982	5.728	4.733
12	Band-Pass Filter	6.982	5.728	4.734

Table 7.2.5: Confrontation of the measured and theoretical values of the RF reception path noise figure.

Operating Mode	**Theoretical Noise Figure [dB]**	**Measured Noise Figure [dB]**	**Error [dB]**
Close Range	6.982	7.234	0.25
Mid Range	5.728	5.944	0.22
Far Range	4.734	4.946	0.21

Chapter 8

Conclusion and Outlook

8.1 Conclusions

The power level plan, as presented in this work, represents the most important step of the design process of the system back-end. This procedure allowed us to considerer all the requirements given by the entire radar system and estimates in an exceptionally accurate way all the parameters and characteristic of the transmission and reception path that had to be fulfilled by the components that constitute the system back-end. The power level plan also facilitated the hard task of searching for suitable components, by highlighting just the important parameters that had to be considered, so the system requirements will be satisfied.

Based in the results obtained from the transmitter prototype, presented in section 7.2, it was possible to show that a demonstrator of the transmitter is feasible to build using COTS components. This demonstrator generated enough signal power to feed the front-end system, saturating all the T/R-modules involved in the antenna array, regardless of the square root tapering produced by the feeding network. This demonstrator was designed and tested under the conditions that the RF source generates the sinusoidal 3 GHz signal with a power level of 0 dBm. However, as a result of the implementation of COTS components, the transmitter model presented in this thesis provides certain flexibility on what the RF signal power level that can be generated concerns (Table 4.3.1).In other words, a range of power signal

levels to choose from is available, that satisfy the system front-end power requirements for the correct functioning of the radar system. This range could be larger if the signal power level generated by the RF source was not at the same time the signal used as the local oscillator signal for the down-conversion (I&Q demodulator).

On the other hand, concerning the receiver prototype, it was shown by the previous results presented that, as in the case of the transmitter, the construction of a valid COTS-based demonstrator was achievable, providing the necessary gain to exploit as much as possible the linear dynamic range of the most critical receiver component, the analog-to-digital converter. This is due to the incorporation of a digital attenuator on the reception path, which allows to fix the reception gain for the different requirements demanded for the radar system.

Unfortunately in this case the construction of the entire receiver demonstrator could not be completely COTS-based due to the active differential input/single-ended output low pass filter required and a specific design was generated. Regarding this filter, it is possible to conclude that the Butterworth approximation used for the active filter design is an optimum tool that allows to generate optimum filters whose behavior approximates the characteristics of the ideal filter. The higher is the order of the filter; the better is the resemblance between the designed and the ideal filter. However, there exists a trade-off between the filter's order, the filter construction complexity and the delay produced by the filter. The higher the order of the filter required, the higher the number of operational amplifiers for its construction and a larger delay will be presented at its output with respect to its input. For the particular case of this system back-end, the use of a fifth order Butterworth low pass filter gave a reasonable approximation of the ideal filter, not requiring a higher order filter. As the delay produced by the implementation of this filter is the same for all the received pulses, it use does not affect the global radar system operation.

The system back-end, as mentioned before, has no restriction on its dimension. It is obvious that the transmitter and receiver prototype here constructed could be categorized as non practical as due to their large dimensions. However, it has to be kept in mind that all the components used for the receiver and the transmitter (except for the ADC) were used with

their respective evaluation boards, which means that the final transceiver that will be manufactured will exhibit dimension considerably reduced with respect to this prototype as all the components can be assembled together on just one printed circuit board. This fact will reduce also the losses due to connectors, cables and adaptors which were required for the prototype construction.

For the noise figure measurement procedure it is important to remark how the incorporation of isolators or attenuators in the measurement set-up helps making the measurements more accurate. Using the original Y-factor method to measure noise figure, without the set-up modification presented in this work, will provide valid noise figure results but with a bigger uncertainty than the ones obtained along this thesis.

About the binary phased pulse compression sequences, it is possible to conclude that for code lengths larger than 40 it is recommended to use different approaches to develop the search algorithms for these codes, as the exhaustive search is no longer recommended due to the required huge computation times. The evolutionary algorithm approach used in this thesis gives to the programmer the opportunity to obtain near optimum results without investing too much time. However, depending of the computation time restrictions and the specific purpose of the searched codes, it seems that some improvements can be done to this algorithm in order to obtain better results and to find a larger collection of sequences. For the goal of this thesis the results obtain are considered adequate.

Most of the analysis involved in the generation of the binary phased sequences required by pulse compression technique, is shown in Chapter 6. Nevertheless, it is important to comment that in the case of the cross-correlation analysis it must be remembered that the maximum possible cross-correlation isolation was searched so the minimum interference between codes is produced. In the case of the 32 length optimum sequences found in section 6.2 the minimum possible cross-correlation level between these codes was equal to 7. Therefore these codes have a minimum PSR of -13.2 dB. On the other hand, the near optimum 80 length codes found exhibit a minimum cross-correlation level of 13 which means a PSR of -15.78 dB. Due to the properties of the 80 length codes, these provide higher cross-correlation isolation in comparison with the 32 length codes. However, as 80 length

sequences with lower maximum autocorrelation sidelobe level are possible to find, higher cross-correlation isolation may be possible to get.

8.2 Future Improvements and Work Involving the System Back-End

Several improvements and tests can be carry out as the system back-end design and prototype construction are not yet finished due to time limitations of the work involved in this master thesis.

First of all, the manufacturing and measurement of the designed active differential input/single-ended output low pass filter must be done. Depending on the measurement results of this filter some improvements in the design may be required.

Second of all, involving the I&Q demodulator a particular analysis must be performed in order to continue with the development of the system back-end. As the balun available for the base-band ports on the evaluation board will be take off and substituted by the designed active differential input/single-end output low pass filter, the DC-offset at the differential outputs of the I&Q demodulator must be measured and evaluated to consider if these DC levels will represent a problem to the filter. If this is the case, some improvement or a complete re-design must be performed for the low pass filter.

The complete back-end reception path (from the T/R switch until the ADC) must be then assembled and tested, verifying that the linear dynamic range of the prototype approaches in an acceptable way the theoretical one given by the PLP. In addition the down-conversion, and the low pass filtering must be checked so they maintain the signal to noise ratio available at the I&Q demodulator input.

In the transmitter case the use of two switches (T/R and Shape switches), that turn off the signal generated by the RF source (while the system works in reception mode) have been included in the transmission path. The sum of isolation given for these two switches may not be enough to avoid interference provoked by the RF source during reception. Common radar

systems use magic-Ts, adding more losses and the isolation still could not be enough. If this is the case, one simple solution that can be included in the system back-end is to turn off one or both of the amplifiers placed along the transmission path. In this way the signal power level that cannot be attenuated by the parameters of the COTS components, at least will not be amplified.

During the conception of the RASKEL project design, several assumptions have been made in order to make the design process easier. Between those there is one assumption in particular that is necessary to take into account for the back-end system, due to the fact that it generates considerable losses. For the analysis of the system has always been considered that the amplitude of the pulses (of the same pulse train) coming from one particular target is always the same and that the sampled (at 10MHz) output signal of these pulses is consistently the peak value. In practice this is not strictly true, hence it is produced a degradation of the SNR known as straddling losses. In future improvements of the system back-end these particular types of losses (which were neglected for the purpose of this thesis) should be considered. It could be possible to compensate the straddling losses by adding more gain to the reception path. However, sampling the signals to a higher rate could be other possible way to compensate these losses as some averaging or amplitude selection can be made with the extra samples.

Regarding the binary phased codes, some improvements can be made to the evolutionary algorithm in order to find a larger collection of 80 length pulse compression sequences. Once all the 32 and 80 length sequences are definitely chosen, an FPGA with all of them must produce the BPSK modulation in the transmitter prototype.

The entire receiver must be re-analyzed and improved taking into account the third-order interception point (IP_3 or TOI) which for the matters of this thesis has not been considered. This analysis it is important for further improvement of the system as it considers the interferences due to intermodulation distortion (IMD).

It is significant to mention that Fraunhofer FHR, based on the results and the analysis presented in this thesis, will execute the first practical tests of the novel system back-end demonstrator during the summer of 2011. For the matter of these tests the power level plan will be slightly modified as the

system front-end will be replaced by a rotating antenna. This experiment has the aim of verifying the correct transmission and reception of all the different pulse shapes involved in this system, and the correct detection of some sample targets.

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ANNEX

A. Datasheets

Surface Mount

Monolithic Amplifier

DC-7 GHz

Features

- Miniature SOT-89 Package
- Frequency range, DC to 7 GHz
- Internally Matched to 50 Ohms
- Output power, 10.5 dBm typ.
- Excellent package for heat dissipation, exposed metal bottom
- Aqueous washable
- Protected by US Patent 6,943,629

Applications

- Cellular
- PCS
- Communication receivers & transmitters

Gali 39+

CASE STYLE: DF782
PRICE: $1.19 ea. QTY. (30)

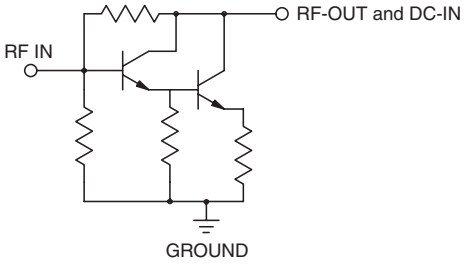
+ RoHS compliant in accordance with EU Directive (2002/95/EC)

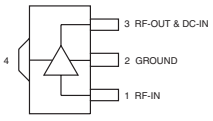
The +Suffix has been added in order to identify RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

General Description

Gali 39+ (RoHS compliant) is a wideband amplifier offering high dynamic range. Lead finish is SnAgNi. It has repeatable performance from lot to lot, and is enclosed in a SOT-89 package. It uses patented Transient Protected Darlington configuration and is fabricated using InGaP HBT technology. Expected MTBF is 4,000 years at 85°C case temperature. Gali 39+ is designed to be rugged for ESD and supply switch-on transients.

simplified schematic and pin description





Function	Pin Number	Description
RF IN	1	RF input pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation.
RF-OUT and DC-IN	3	RF output and bias pin. DC voltage is present on this pin; therefore a DC blocking capacitor is necessary for proper operation. An RF choke is needed to feed DC bias without loss of RF signal due to the bias connection, as shown in "Recommended Application Circuit".
GND	2,4	Connections to ground. Use via holes as shown in "Suggested Layout for PCB Design" to reduce ground path inductance for best performance.

Electrical Specifications at 25°C and 35mA, unless noted

Parameter		Min.	Typ.	Max.	Units
Frequency Range*		DC		7	GHz
Gain	f=0.1 GHz		20.8		dB
	f=1 GHz		21.1		
	f=2 GHz	17.7	19.7		
	f=3 GHz		17.7		
	f=4 GHz		17.0		
	f=5 GHz		16.1		
	f=7 GHz		17.6		
	f=10 GHz		9.8		
Input Return Loss	f= DC to 3 GHz		12.5		dB
	f= 3 to 7 GHz		11		
Output Return Loss	f= DC to 3 GHz		14		dB
	f= 3 to 7 GHz		8.0		
Output Power @ 1 dB compression	f=7 GHz	9.0	10.5		dBm
Output IP3	f=2 GHz		22.9		dBm
Noise Figure	f=2 GHz		2.4		dB
Recommended Device Operating Current			35		mA
Device Operating Voltage		3.1	3.5	3.9	V
Device Voltage Variation vs. Temperature at 35 mA			-2.5		mV/°C
Device Voltage Variation vs. Current at 25°C			2.9		mV/mA
Thermal Resistance, junction-to-case[1]			350		°C/W

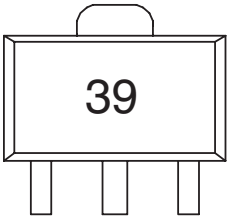
*Guaranteed specification DC-7 GHz. Low frequency cut off determined by external coupling capacitors.

Absolute Maximum Ratings

Parameter	Ratings
Operating Temperature*	-45°C to 85°C
Storage Temperature	-65°C to 150°C
Operating Current	55mA
Input Power	13dBm

Note: Permanent damage may occur if any of these limits are exceeded.
These ratings are not intended for continuous normal operation.
[1]Case is defined as ground leads.
*Based on typical case temperature rise 2°C above ambient.

Product Marking



Additional Detailed Technical Information

Additional information is available on our web site. To access this information enter the model number on our web site home page.

Performance data, graphs, s-parameter data set (.zip file)

Case Style: DF782

Plastic package, exposed paddle, lead finish: tin/silver/nickel

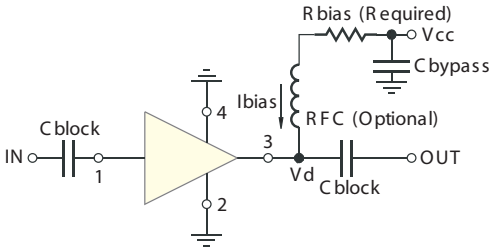
Tape & Reel: F55

Suggested Layout for PCB Design: PL-019

Evaluation Board: TB-409-39+

Environmental Ratings: ENV08T2

Recommended Application Circuit



Test Board includes case, connectors, and components (in bold) soldered to PCB

R BIAS	
Vcc	**"1%" Res. Values (ohms) for Optimum Biasing**
7	107
8	133
9	162
10	191
11	221
12	249
13	280
14	309
15	340
16	365
17	392
18	422
19	453
20	475

ESD Rating

Human Body Model (HBM): Class 1A (250V to < 500V) in accordance with ANSI/ESD STM 5.1 - 2001

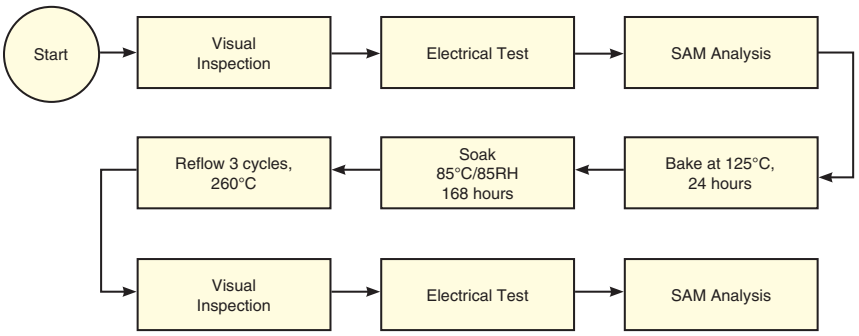
Machine Model (MM): Class M1 (< 100V) in accordance with ANSI/ESD STM 5.2 - 1999

MSL Rating

Moisture Sensitivity: MSL1 in accordance with IPC/JEDECJ-STD-020C

No.	Test Required	Condition	Standard	Quantity
1	Visual Inspection	Low Power Microscope Magnification 40x	MIP-IN-0003 (MCT spec)	45 units
2	Electrical Test	Room Temperature	SCD (MCL spec)	45 units
3	SAM Analysis	Less than 10% growth in term of delamination	J-Std-020C (Jedec Standard)	45 units
4	Moisture Sensitivity Level 1	Bake at 125°C for 24 hours Soak at 85°C/85%RH for 168 hours Reflow 3 cycles at 260°C peak	J-Std-020C (Jedec Standard)	45 units

MSL Test Flow Chart



Limiter

RLM-33+

50Ω Broadband 30 to 3000 MHz

CASE STYLE: TT1224

The Big Deal

- Wide Frequency range 30 to 3000 MHz
- Excellent limiting beyond +12 dBm input power
- Very quick recovery time, 10 nsec
- Low insertion loss, 0.23 dB

Product Overview

The RLM-33+ is packaged in a miniature size (0.25 X 0.3 in.) and protects against ESD and input power surges over a frequency range 30 to 3000 MHz. Construction is on a micro strip low loss dielectric material and cased into Mini-Circuits high volume, low cost “R” package for cost efficiencies.

The RLM-33+ limiter provides excellent protection of low noise amplifiers in hostile environments where unwanted signals prevail such as in manufacturing sites, train tunnels, etc.

Key Features

Feature	Advantages
Limiting abilities from +12 to +30 dBm	Protects against strong undesired signals and prevents burn out of amplifiers
Frequency coverage 30 to 3000 MHz	Protects against many different types of unwanted signals including ESD
Surface mount package, miniature size	Allows convenient placement in amplifiers incorporating this protective device
Low insertion loss and VSWR	Provides minimal degradation to amplifier performance, especially for low noise amplifiers where input loss is critical
Low Cost	A practical solution to incorporate into amplifier design with a minimal affect on cost

Surface Mount

Limiter

50Ω Broadband 30 to 3000 MHz

RLM-33+

CASE STYLE: TT1224
PRICE: $9.95 ea. QTY (10-49)

+ RoHS compliant in accordance with EU Directive (2002/95/EC)

The +Suffix has been added in order to identify RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

Maximum Ratings

Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 100°C
RF Input Power	2W

Permanent damage may occur if any of these limits are exceeded.

Pin Connections

INPUT	1
OUTPUT	4
GROUND	2,3,5,6

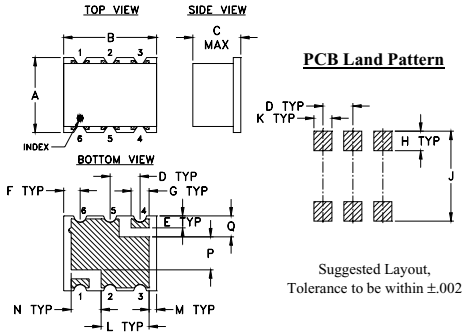
Features

- wideband, 30 to 3000 MHz
- low insertion loss 0.23 dB typ.
- fast recovery time, 10nsec typ.
- excellent VSWR 1.05:1 typ.
- low leakage power, 11.5 dBm typ.

Applications

- military, hi-rel applications
- stabilizing generator outputs
- reducing amplitude variations
- protects low noise amplifiers and other devices from ESD or input power damage

Outline Drawing



Suggested Layout, Tolerance to be within ±.002

Outline Dimensions (inch / mm)

A	B	C	D	E	F	G	H
.25	.31	.16	.100	.040	.055	.060	.065
6.35	7.87	4.06	2.54	1.02	1.40	1.52	1.65

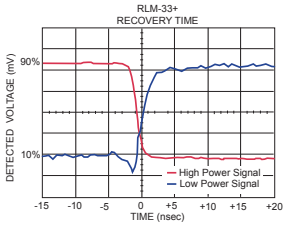
J	K	L	M	N	P	Q	wt.
.300	.060	.160	.025	.100	.110	.070	grams
7.62	1.52	4.06	0.64	2.54	2.79	1.78	0.16

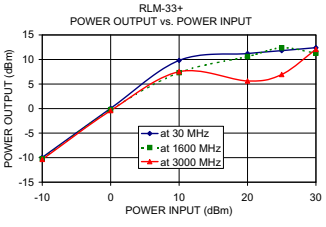
Electrical Specifications

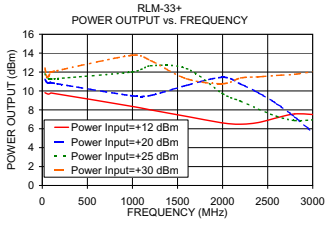
Parameter	Condition	Min.	Typ.	Max.	Units
Frequency Range		30		3000	MHz
Insertion Loss in Linear Range	<+5 dBm Input	—	0.23	0.7	dB
VSWR	<+5 dBm Input	—	1.05	1.5	:1
Input Power Range	Output Power Limited	+12	—	+30	dBm
Output Power	In limiting range	—	+11.5	—	dBm
Recovery Time	1 watt pulse 50 µsec pw 1kHz duty cycle recovery to within 90% of final value.	—	10	—	nsec
Response Time	-30 to +30 dBm input 50 µsec, BW 1 kHz duty cycle	—	2	—	nsec
Limiting Δ Output/1dB Δ Input	Input Power Range (dBm) 12 to 20 20 to 25 25 to 30	—	 0.2 0.2 0.2	—	dB/dB

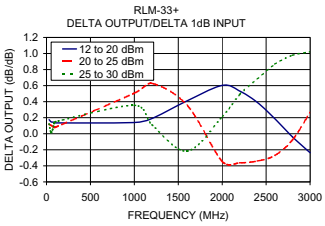
Typical Performance Data

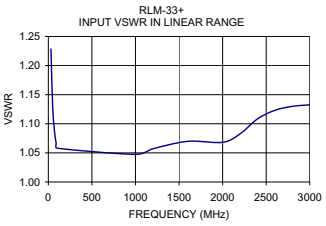
Freq. (MHz)	I. Loss in Linear Range (dB)	VSWR in Linear Range (:1)	Power Output (dBm) +12dBm Input	Power Output (dBm) +20dBm Input	Power Output (dBm) +25 dBm Input	Power Output (dBm) +30dBm Input	Δ Output 1dB Δ Input +12 to +20dBm Input	Δ Output 1dB Δ Input +20 to +25 dBm Input	Δ Output 1dB Δ Input +25 to +30 dBm Input
30.00	0.08	1.23	9.81	11.21	11.80	12.41	0.18	0.12	0.12
50.00	0.06	1.13	9.72	10.92	11.45	11.53	0.15	0.11	0.02
70.00	0.06	1.09	9.66	10.82	11.28	11.54	0.15	0.09	0.05
90.00	0.06	1.07	9.75	10.90	11.29	11.98	0.14	0.08	0.14
100.00	0.06	1.06	9.78	10.86	11.26	12.01	0.14	0.08	0.15
1000.00	0.22	1.05	8.36	9.48	12.01	13.78	0.14	0.51	0.35
1200.00	0.23	1.06	8.00	9.52	12.66	13.22	0.19	0.63	0.11
1600.00	0.29	1.07	7.31	10.59	12.37	11.29	0.41	0.36	-0.22
2000.00	0.32	1.07	6.62	11.44	9.71	10.77	0.60	-0.35	0.21
2200.00	0.34	1.08	6.48	10.73	8.92	11.37	0.53	-0.36	0.49
2400.00	0.39	1.11	6.66	9.78	8.08	11.49	0.39	-0.34	0.68
2600.00	0.40	1.12	7.16	8.65	7.30	11.64	0.19	-0.27	0.87
2800.00	0.41	1.13	7.57	7.25	6.87	11.76	-0.04	-0.08	0.98
3000.00	0.43	1.13	7.51	5.62	6.94	12.05	-0.24	0.26	1.02

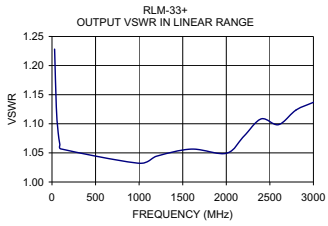




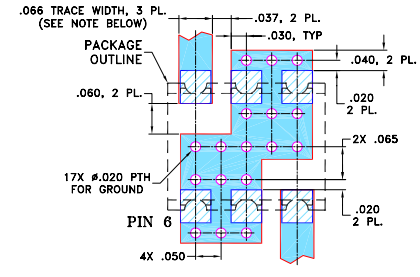








Demo Board MCL P/N: TB-393
Suggested PCB Layout (PL-258)



NOTES: 1. TRACE WIDTH IS SHOWN FOR ROGERS RO4350B WITH DIELECTRIC THICKNESS .030" ± .002"; COPPER: 1/2 OZ. EACH SIDE. FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED.
2. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.

DENOTES PCB COPPER LAYOUT WITH SMOBC (SOLDER MASK OVER BARE COPPER)

DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK

Ceramic

Bandpass Filter

BFCN-3010+

50Ω 2920 to 3100 MHz

CASE STYLE: FV1206
PRICE: $3.95 ea. QTY (10-49)

+ RoHS compliant in accordance with EU Directive (2002/95/EC)

The +Suffix has been added in order to identify RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

Maximum Ratings

Operating Temperature	-55°C to 100°C
Storage Temperature	-55°C to 100°C
RF Power Input*	1.5W at 25°C

*Passband rating, derate linearly to 0.25W at 100°C ambient
Permanent damage may occur if any of these limits are exceeded.

Pin Connections

RF IN	1
RF OUT	3
GROUND	2,4

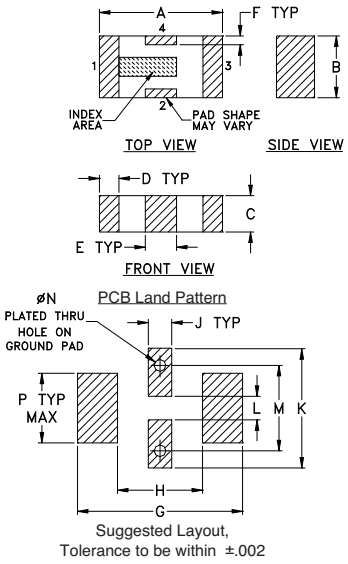
Features

- Good VSWR, 1.6:1 typ @ passband
- Small size
- Temperature stable
- LTCC construction

Applications

- Harmonic rejection
- Transmitters / receivers
- Wireless transceiver
- Point-to-point communications
- Radio location

Outline Drawing



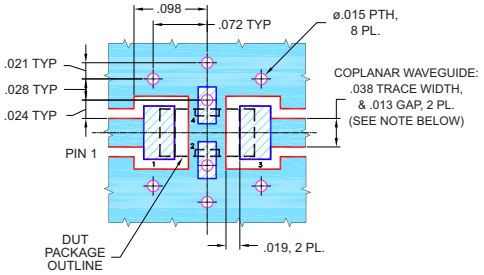
Suggested Layout,
Tolerance to be within ±.002

Outline Dimensions (inch / mm)

A	B	C	D	E	F	G	H
.126	.063	.037	.020	.032	.009	.169	.087
3.20	1.60	0.94	0.51	0.81	0.23	4.29	2.21

J	K	L	M	N	P	WT.
.024	.122	.024	.087	.012	.071	GRAM
0.61	3.10	0.61	2.21	0.30	1.80	.020

Demo Board MCL P/N: TB-270
Suggested PCB Layout (PL-137)



NOTES:

1. COPLANAR WAVEGUIDE PARAMETERS ARE SHOWN FOR ROGERS RO4350B WITH THICKNESS .020" ± .0015".
   COPPER: 1/2 OZ. EACH SIDE.
   FOR OTHER MATERIALS TRACE WIDTH & GAP MAY NEED TO BE MODIFIED.
2. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.

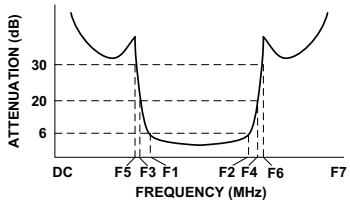
DENOTES PCB COPPER LAYOUT WITH SMOBC (SOLDER MASK OVER BARE COPPER)

DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK

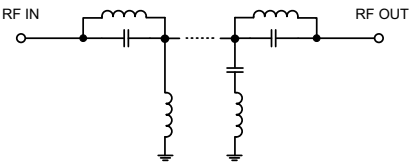
Electrical Specifications at 25°C

Parameter		F#	Frequency (MHz)	Min.	Typ.	Max.	Unit
Pass Band	Center Frequency				3010		MHz
	Insertion Loss	F1-F2	2920-3100			6	dB
	VSWR	F1-F2	2920-3100		1.6	3.0	:1
Stop Band, Lower	Insertion Loss	DC-F5	DC-1300		30		dB
		DC-F3	DC-1530	20			dB
	VSWR	DC-F3	DC-1530		20		:1
Stop Band, Upper	Insertion Loss	F4-F6	4450-4650	20			dB
		F6-F7	4650-6600		30		dB
	VSWR	F4-F7	4450-6600		20		:1

Typical Frequency Response



Functional Schematic

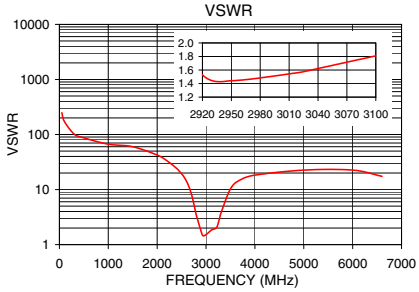


Typical Performance Data at 25°C

Frequency (MHz)	Insertion Loss (dB)	VSWR (:1)
50	86.94	248.17
500	48.07	86.86
1300	31.07	62.05
1530	28.16	57.91
2700	18.27	8.31
2800	7.88	3.46
2920	3.03	1.53
3000	2.73	1.50
3010	2.56	1.53
3050	2.92	1.66
3100	3.15	1.83
3200	5.82	1.98
3250	10.05	2.45
3400	19.93	7.08
4100	28.17	18.50
4450	29.63	19.87
4650	34.88	20.70
5600	28.64	23.81
6600	29.26	17.39

BFCN-3010+
INSERTION LOSS

BFCN-3010+
VSWR



For detailed performance specs & shopping online see web site

REV. OR
M123626
EDR-9332/1F1
BFCN-3010+
RAV
090721

400 MHz to 6 GHz Quadrature Demodulator

ADL5380

FEATURES

Operating RF and LO frequency: 400 MHz to 6 GHz
Input IP3
30 dBm @ 900 MHz
28 dBm @1900 MHz
Input IP2: >65 dBm @ 900 MHz
Input P1dB (IP1dB): 11.6 dBm @ 900 MHz
Noise figure (NF)
10.9 dB @ 900 MHz
11.7 dB @ 1900 MHz
Voltage conversion gain: ~7 dB
Quadrature demodulation accuracy @ 900 MHz
Phase accuracy: ~0.2°
Amplitude balance: ~0.07 dB
Demodulation bandwidth: ~390 MHz
Baseband I/Q drive: 2 V p-p into 200 Ω
Single 5 V supply

FUNCTIONAL BLOCK DIAGRAM

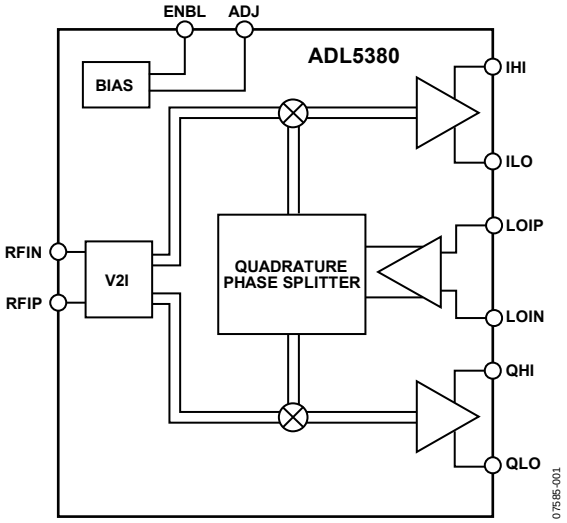


Figure 1.

APPLICATIONS

Cellular W-CDMA/GSM/LTE
Microwave point-to-(multi)point radios
Broadband wireless and WiMAX

GENERAL DESCRIPTION

The ADL5380 is a broadband quadrature I-Q demodulator that covers an RF/IF input frequency range from 400 MHz to 6 GHz. With a NF = 10.9 dB, IP1dB = 11.6 dBm, and IIP3 = 29.7 dBm @ 900 MHz, the ADL5380 demodulator offers outstanding dynamic range suitable for the demanding infrastructure direct-conversion requirements. The differential RF inputs provide a well-behaved broadband input impedance of 50 Ω and are best driven from a 1:1 balun for optimum performance.

Excellent demodulation accuracy is achieved with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively. The demodulated in-phase (I) and quadrature (Q) differential outputs are fully buffered and provide a voltage conversion gain of ~7 dB. The buffered baseband outputs are capable of driving a 2 V p-p differential signal into 200 Ω.

The fully balanced design minimizes effects from second-order distortion. The leakage from the LO port to the RF port is <−50 dBm. Differential dc offsets at the I and Q outputs are typically <20 mV. Both of these factors contribute to the excellent IIP2 specification, which is >65 dBm.

The ADL5380 operates off a single 4.75 V to 5.25 V supply. The supply current is adjustable by placing an external resistor from the ADJ pin to either the positive supply, V_S, (to increase supply current and improve IIP3) or to ground (which decreases supply current at the expense of IIP3).

The ADL5380 is fabricated using the Analog Devices, Inc., advanced silicon-germanium bipolar process and is available in a 24-lead exposed paddle LFCSP.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

7/09—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, f_{LO} = 900 MHz, f_{IF} = 4.5 MHz, P_{LO} = 0 dBm, Z_O = 50 Ω, unless otherwise noted. Baseband outputs differentially loaded with 450 Ω. Loss of the balun used to drive the RF port was de-embedded from these measurements.

Table 1.

Parameter	Condition	Min	Typ	Max	Unit
OPERATING CONDITIONS					
LO and RF Frequency Range		0.4		6	GHz
LO INPUT	LOIP, LOIN				
Input Return Loss	LO driven differentially through a balun at 900 MHz		−10		dB
LO Input Level		−6	0	+6	dBm
I/Q BASEBAND OUTPUTS	QHI, QLO, IHI, ILO				
Voltage Conversion Gain	450 Ω differential load on I and Q outputs at 900 MHz		6.9		dB
	200 Ω differential load on I and Q outputs at 900 MHz		5.9		dB
Demodulation Bandwidth	1 V p-p signal, 3 dB bandwidth		390		MHz
Quadrature Phase Error	At 900 MHz		0.2		Degrees
I/Q Amplitude Imbalance			0.07		dB
Output DC Offset (Differential)	0 dBm LO input at 900 MHz		±10		mV
Output Common Mode	Dependent on ADJ pin setting				
	V_{ADJ} ~ 4 V (set by 1.5 kΩ from ADJ pin to V_S)		V_S − 2.5		V
	V_{ADJ} ~ 4.8 V (set by 200 Ω from ADJ pin to V_S)		V_S − 2.8		V
	V_{ADJ} ~ 2.4 V (ADJ pin open)		V_S − 1.2		V
0.1 dB Gain Flatness			37		MHz
Output Swing	Differential 200 Ω load		2		V p-p
Peak Output Current	Each pin		12		mA
POWER SUPPLIES	V_S = VCC1, VCC2, VCC3				
Voltage		4.75		5.25	V
Current	1.5 kΩ from ADJ pin to V_S; ENBL pin low		245		mA
	1.5 kΩ from ADJ pin to V_S; ENBL pin high		145		mA
ENABLE FUNCTION	Pin ENBL				
Off Isolation			−70		dB
Turn-On Settling Time	ENBL high to low		45		ns
Turn-Off Settling Time	ENBL low to high		950		ns
ENBL High Level (Logic 1)		2.5			V
ENBL Low Level (Logic 0)				1.7	V
DYNAMIC PERFORMANCE at RF = 900 MHz	V_{ADJ} ~ 4 V (set by 1.5 kΩ from ADJ pin to V_S)				
Conversion Gain			6.9		dB
Input P1dB			11.6		dBm
RF Input Return Loss	RFIP, RFIN driven differentially through a balun		−19		dB
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		68		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		29.7		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω		−52		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−67		dBc
IQ Magnitude Imbalance			0.07		dB
IQ Phase Imbalance			0.2		Degrees
Noise Figure			10.9		dB
Noise Figure Under Blocking Conditions	With a −5 dBm input interferer 5 MHz away		13.1		dB

Parameter	Condition	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE at RF = 1900 MHz	V_{ADJ} ~ 4 V (set by 1.5 kΩ from ADJ pin to V_S)				
Conversion Gain			6.8		dB
Input P1dB			11.6		dBm
RF Input Return Loss	RFIP, RFIN driven differentially through a balun		−13		dB
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		61		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		27.8		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω		−49		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−77		dBc
IQ Magnitude Imbalance			0.07		dB
IQ Phase Imbalance			0.25		Degrees
Noise Figure			11.7		dB
Noise Figure Under Blocking Conditions	With a −5 dBm input interferer 5 MHz away		14		dB
DYNAMIC PERFORMANCE at RF = 2700 MHz	V_{ADJ} ~ 4 V (set by 1.5 kΩ from ADJ pin to V_S)				
Conversion Gain			7.4		dB
Input P1dB			11		dBm
RF Input Return Loss	RFIP, RFIN driven differentially through a balun		−10		dB
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		54		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		28		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω		−49		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−73		dBc
IQ Magnitude Imbalance			0.07		dB
IQ Phase Imbalance			0.5		Degrees
Noise Figure			12.3		dB
DYNAMIC PERFORMANCE at RF = 3600 MHz	V_{ADJ} ~ 4.8 V (set by200 Ω from ADJ pin to V_S)				
Conversion Gain			6.3		dB
Input P1dB			9.6		dBm
RF Input Return Loss	RFIP, RFIN driven differentially through a balun		−11		dB
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		48		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		21		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω		−46		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−72		dBc
IQ Magnitude Imbalance			0.14		dB
IQ Phase Imbalance			1.1		Degrees
Noise Figure			14.2		dB
Noise Figure Under Blocking Conditions	With a −5 dBm input interferer 5 MHz away		16.2		dB
DYNAMIC PERFORMANCE at RF = 5800 MHz	V_{ADJ} ~ 2.4 V (ADJ pin left open)				
Conversion Gain			5.8		dB
Input P1dB			8.2		dBm
RF Input Return Loss	RFIP, RFIN driven differentially through a balun		−7.5		dB
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		44		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		20.6		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω		−47		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−62		dBc
IQ Magnitude Imbalance			0.07		dB
IQ Phase Imbalance			−1.25		Degrees
Noise Figure			15.5		dB
Noise Figure Under Blocking Conditions	With a −5 dBm input interferer 5 MHz away		18.9		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage: VCC1, VCC2, VCC3	5.5 V
LO Input Power	13 dBm (re: 50 Ω)
RF Input Power	15 dBm (re: 50 Ω)
Internal Maximum Power Dissipation	1370 mW
θ_{JA}[1]	53°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C

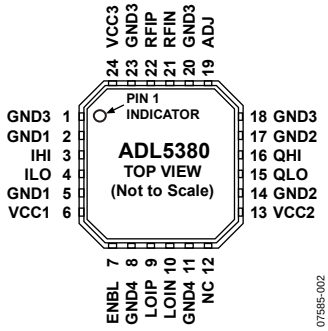
[1] Per JDEC standard JESD 51-2. For information on optimizing thermal impedance, see the Thermal Grounding and Evaluation Board Layout section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD SHOULD BE CONNECTED TO A LOW IMPEDANCE THERMAL AND ELECTRICAL GROUND PLANE.

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 5, 8, 11, 14, 17, 18, 20, 23	GND1, GND2, GND3, GND4	Ground Connect.
3, 4, 15, 16	IHI, ILO, QLO, QHI	I Channel and Q Channel Mixer Baseband Outputs. These outputs have a 50 Ω differential output impedance (25 Ω per pin). Each output pair can swing 2 V p-p (differential) into a load of 200 Ω. The output 3 dB bandwidth is ~400 MHz.
6, 13, 24	VCC1, VCC2, VCC3	Supply. Positive supply for LO, IF, biasing, and baseband sections. Decouple these pins to the board ground using the appropriate-sized capacitors.
7	ENBL	Enable Control. When pulled low, the part is fully enabled; when pulled high, the part is partially powered down and the output is disabled.
9, 10	LOIP, LOIN	Local Oscillator Input. Pins must be ac-coupled. A differential drive through a balun is necessary to achieve optimal performance. Recommended balun is the Mini-Circuits TC1-1-13 for lower frequencies, the Johanson Technology 3600 balun for midband frequencies, and the Johanson Technology 5400 balun for high band frequencies. Balun choice depends on the desired frequency range of operation.
12	NC	Do not connect this pin.
19	ADJ	A resistor to V_S that optimizes third-order intercept. For operation <3 GHz, R_{ADJ} = 1.5 kΩ. For operation from 3 GHz to 4 GHz, R_{ADJ} = 200 Ω. For operation >5 GHz, R_{ADJ} = open. See the Circuit Description section for more details.
21, 22	RFIN, RFIP	RF Input. A single-ended 50 Ω signal can be applied differentially to the RF inputs through a 1:1 balun. Recommended balun is the Mini-Circuits TC1-1-13 for lower frequencies, the Johanson Technology 3600 balun for midband frequencies, and the Johanson Technology 5400 balun for high band frequencies. Balun choice depends on the desired frequency range of operation.
	EP	Exposed Paddle. Connect to a low impedance thermal and electrical ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, LO drive level = 0 dBm, RF input balun loss is de-embedded, unless otherwise noted.

LOW BAND OPERATION

RF = 400 MHz to 3 GHz; Mini-Circuits TC1-1-13 balun on LO and RF inputs, 1.5 kΩ from the ADJ pin to V_S.

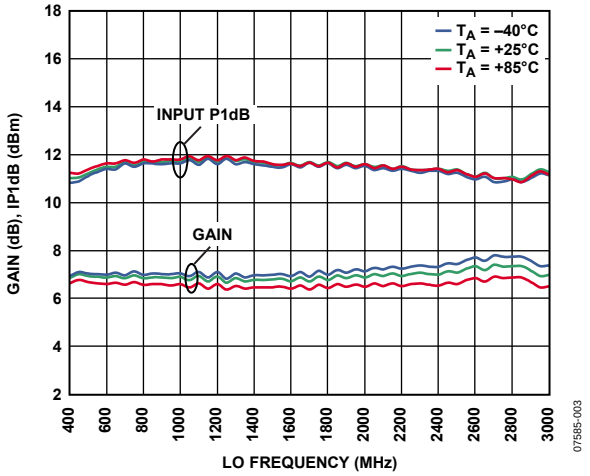


Figure 3. Conversion Gain and Input 1 dB Compression Point (IP1dB) vs. LO Frequency

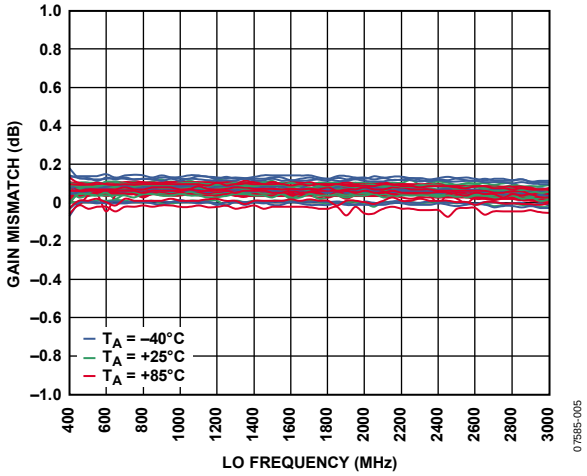


Figure 5. IQ Gain Mismatch vs. LO Frequency

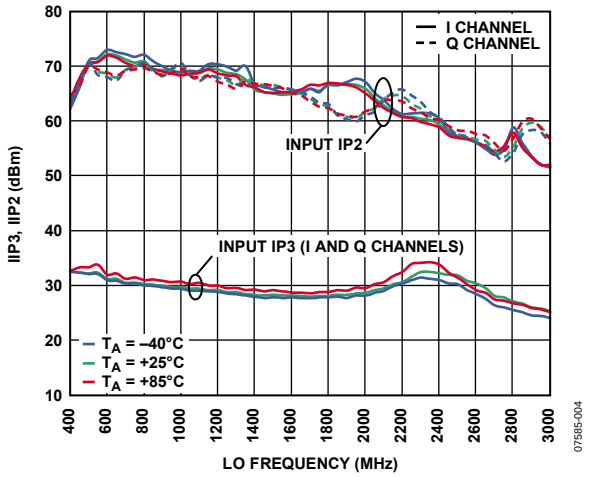


Figure 4. Input Third-Order Intercept (IIP3) and Input Second-Order Intercept Point (IIP2) vs. LO Frequency

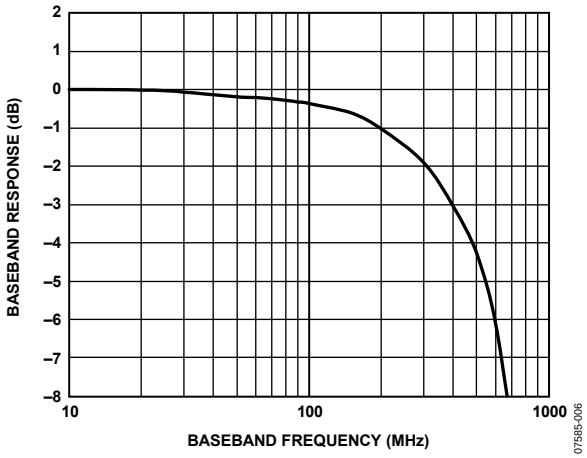


Figure 6. Normalized IQ Baseband Frequency Response

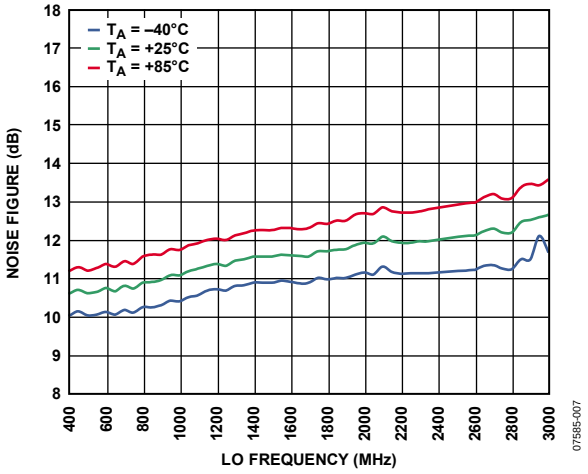


Figure 7. Noise Figure vs. LO Frequency

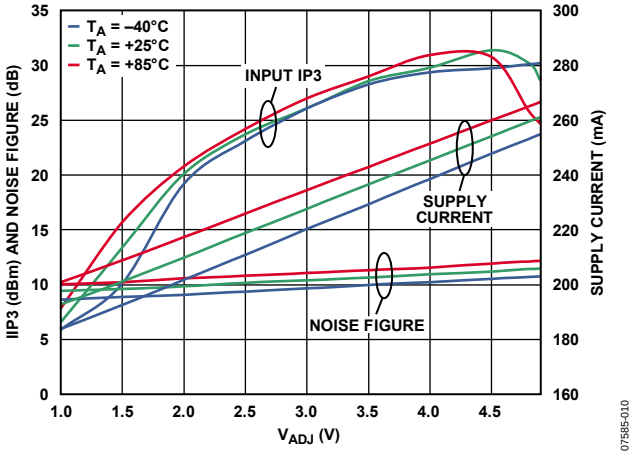


Figure 10. IIP3, Noise Figure, and Supply Current vs. V_{ADJ}, f_{LO} = 900 MHz

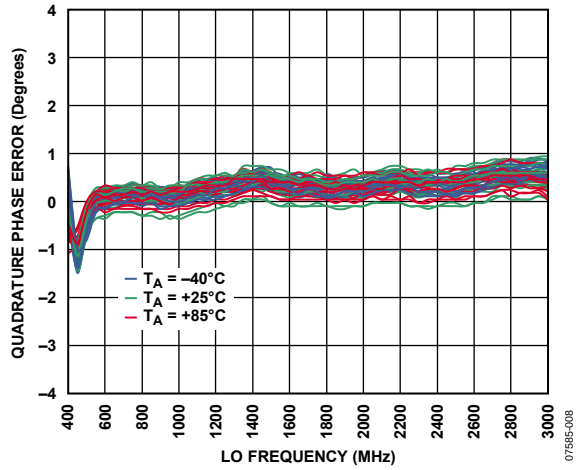


Figure 8. IQ Quadrature Phase Error vs. LO Frequency

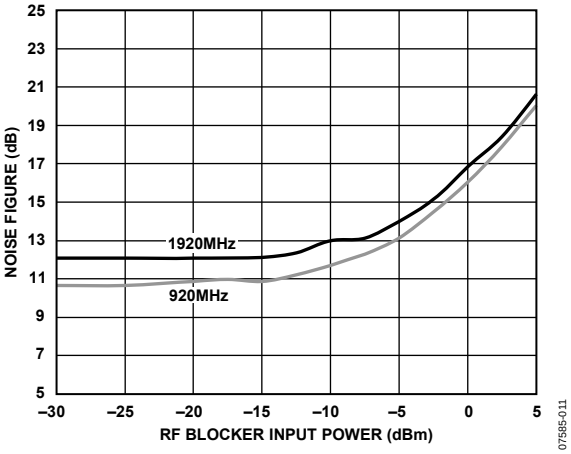


Figure 11. Noise Figure vs. Input Blocker Level, f_{LO} = 900 MHz, f_{LO} = 1900 MHz (RF Blocker 5 MHz Offset)

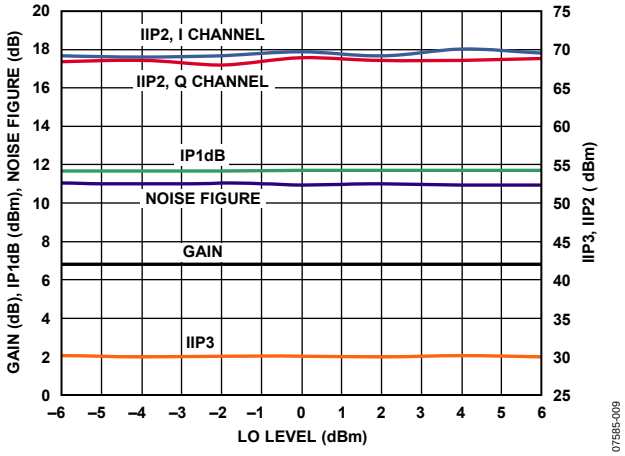


Figure 9. Conversion Gain, IP1dB, Noise Figure, IIP3, and IIP2 vs. LO Level, f_{LO} = 900 MHz

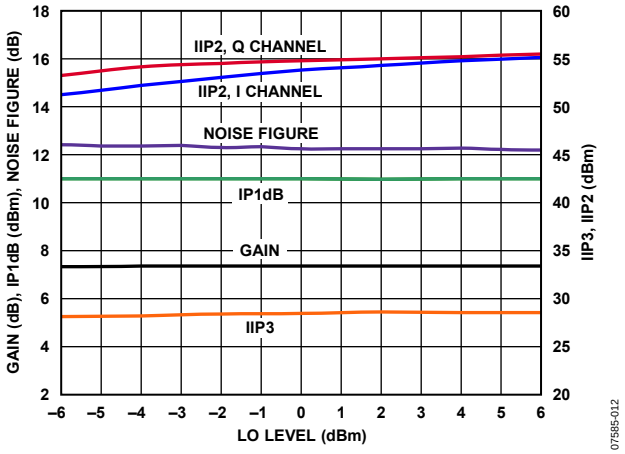


Figure 12. Conversion Gain, IP1dB, Noise Figure, IIP3, and IIP2 vs. LO Level, f_{LO} = 2700 MHz

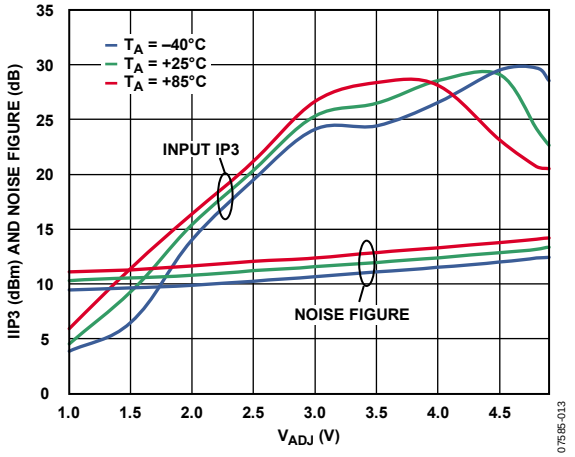


Figure 13. IIP3 and Noise Figure vs. V_{ADJ}, f_{LO} = 2700 MHz

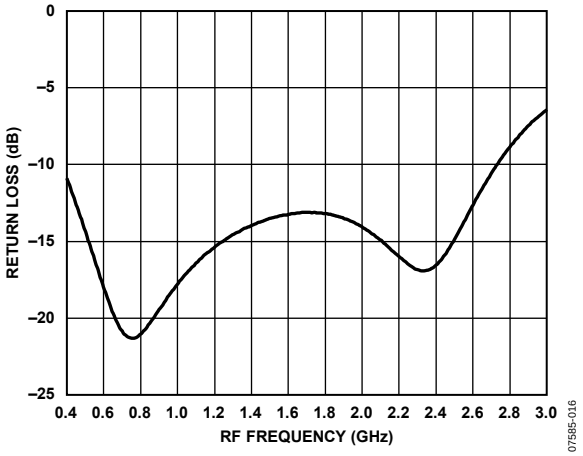


Figure 16. RF Port Return Loss vs. RF Frequency Measured on Characterization Board Through TC1-1-13 Balun

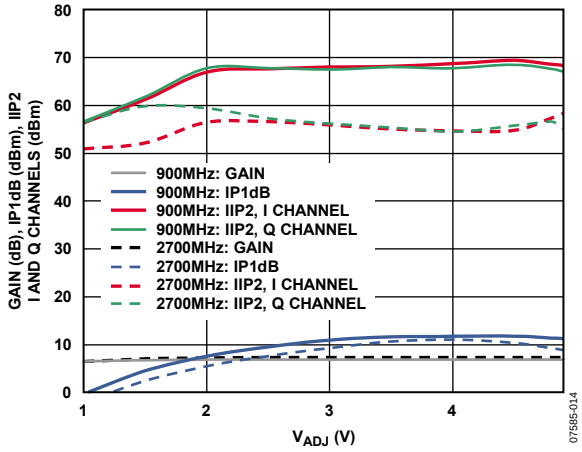


Figure 14. Conversion Gain, IP1dB, and IIP2 vs. V_{ADJ}, f_{LO} = 900 MHz, f_{LO} = 2700 MHz

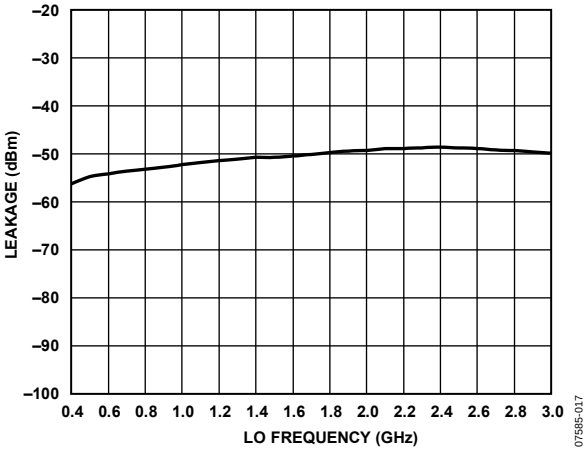


Figure 17. LO-to-RF Leakage vs. LO Frequency

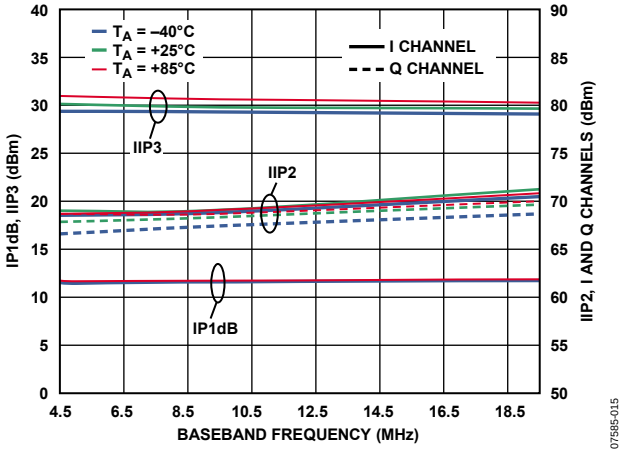


Figure 15. IP1dB, IIP3, and IIP2 vs. Baseband Frequency

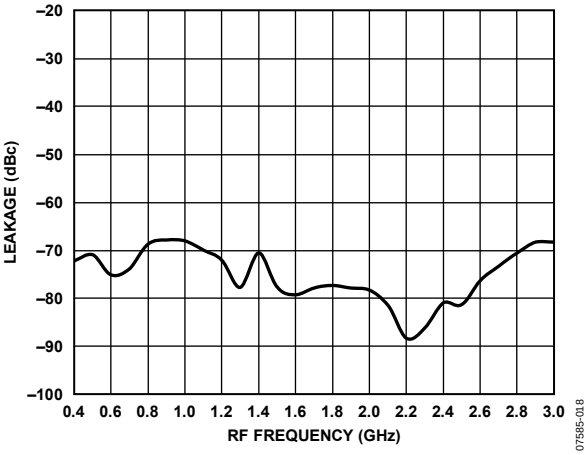


Figure 18. RF-to-LO Leakage vs. RF Frequency

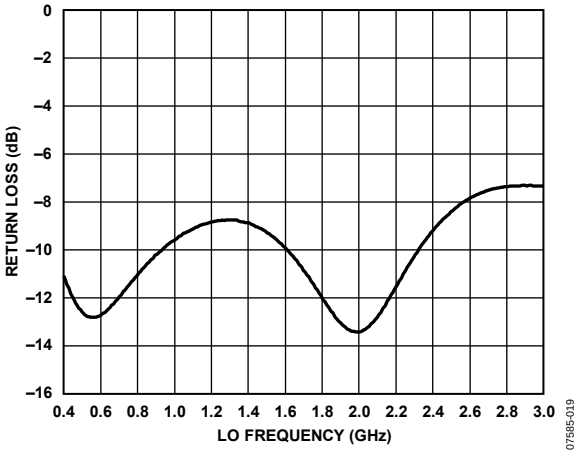


Figure 19. LO Port Return Loss vs. LO Frequency Measured on Characterization Board Through TC1-1-13 Balun

MIDBAND OPERATION

RF = 3 GHz to 4 GHz; Johanson Technology 3600BL14M050T balun on LO and RF inputs, 200 Ω from V_{ADJ} to V_S.

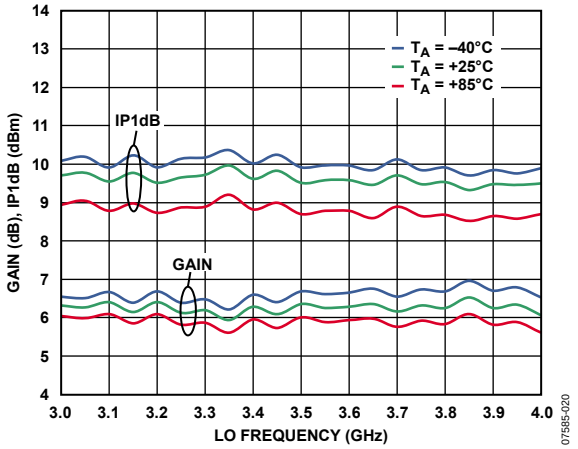


Figure 20. Conversion Gain and Input 1 dB Compression Point (IP1dB) vs. LO Frequency

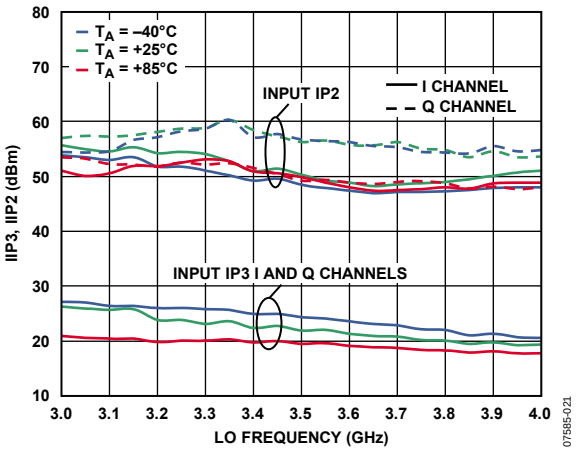


Figure 21. Input Third-Order Intercept (IIP3) and Input Second-Order Intercept Point (IIP2) vs. LO Frequency

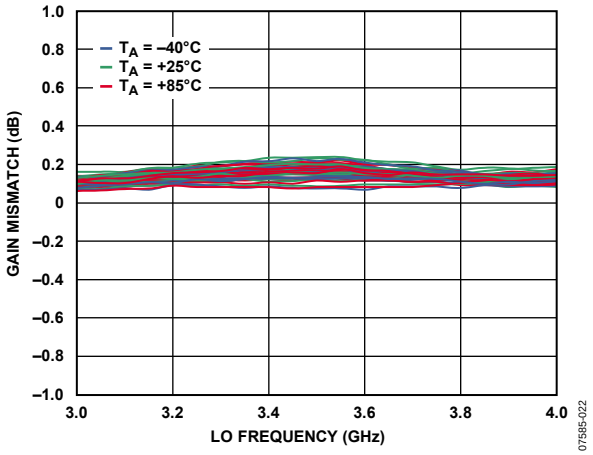


Figure 22. IQ Gain Mismatch vs. LO Frequency

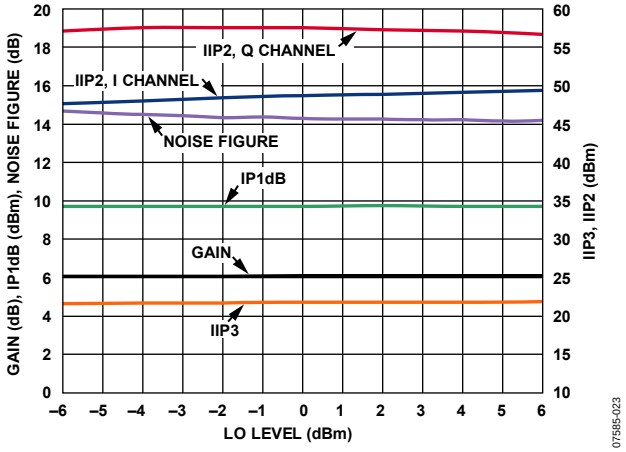


Figure 23. Conversion Gain, IP1dB, Noise Figure, IIP3, and IIP2 vs. LO Level, f_{LO} = 3600 MHz

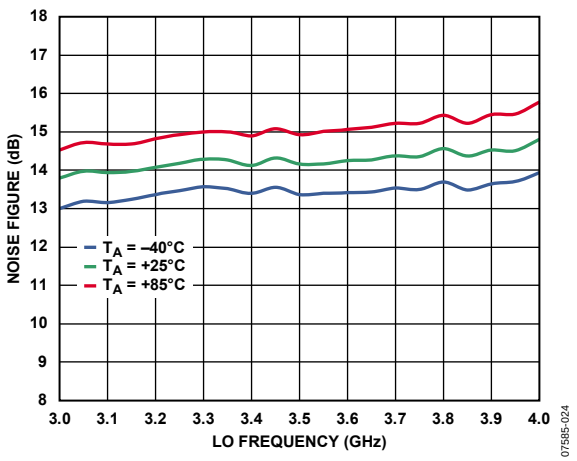


Figure 24. Noise Figure vs. LO Frequency

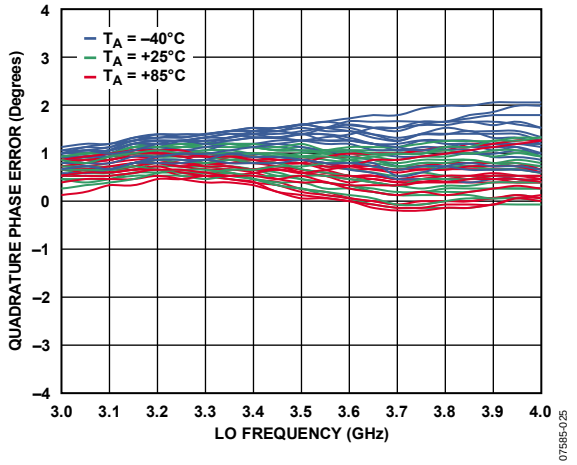


Figure 25. IQ Quadrature Phase Error vs. LO Frequency

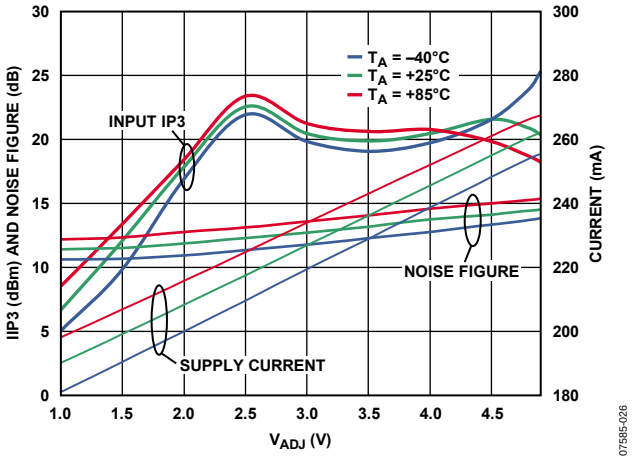


Figure 26. IIP3, Noise Figure, and Supply Current vs. V_{ADJ}, f_{LO} = 3600 MHz

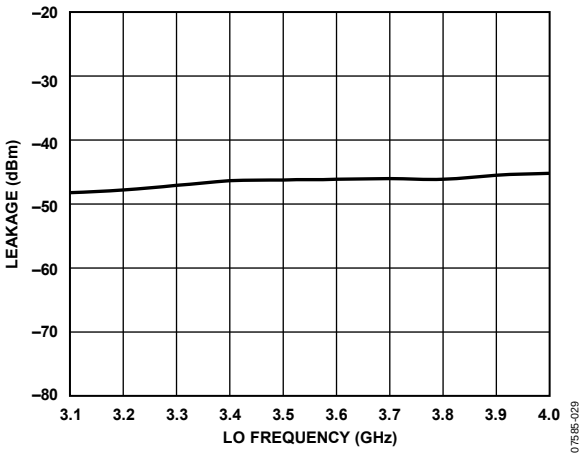


Figure 29. LO-to-RF Leakage vs. LO Frequency

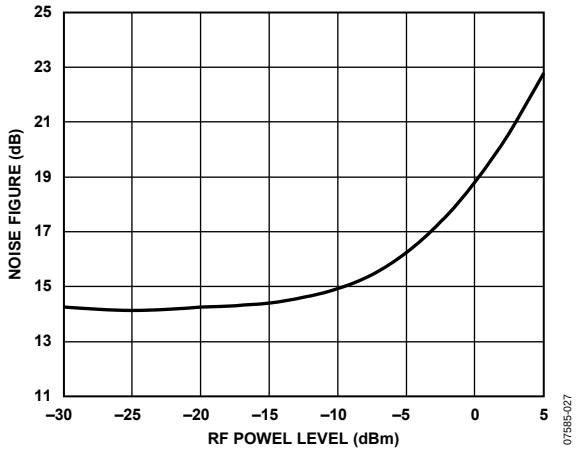


Figure 27. Noise Figure vs. Input Blocker Level, f_{LO} = 3600 MHz (RF Blocker 5 MHz Offset)

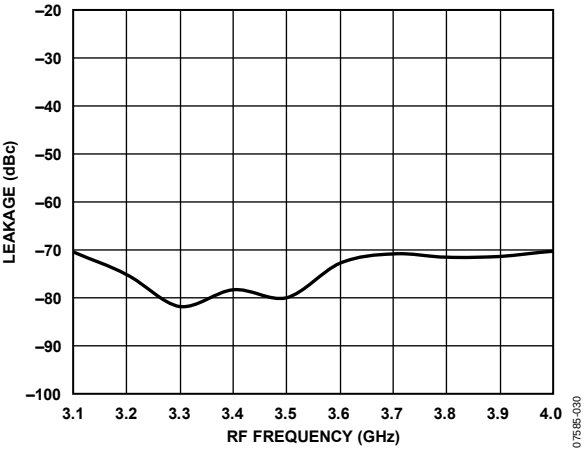


Figure 30. RF-to-LO Leakage vs. RF Frequency

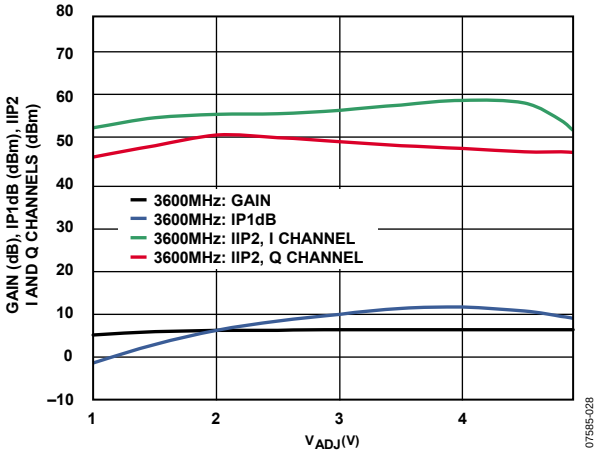


Figure 28. Conversion Gain, IP1dB, and IIP2 vs. V_{ADJ}, f_{LO} = 3600 MHz

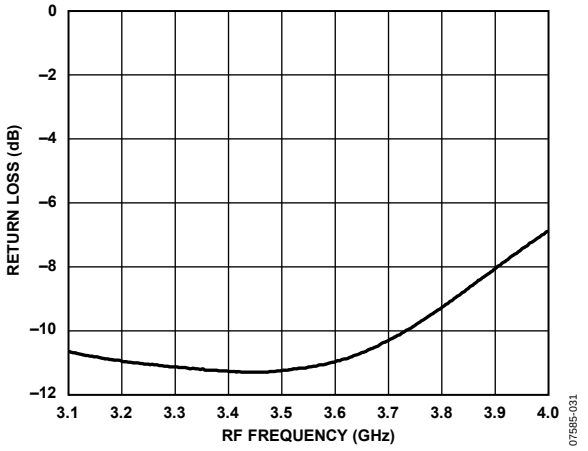


Figure 31. RF Port Return Loss vs. RF Frequency Measured on Characterization Board Through Johanson Technology 3600 Balun

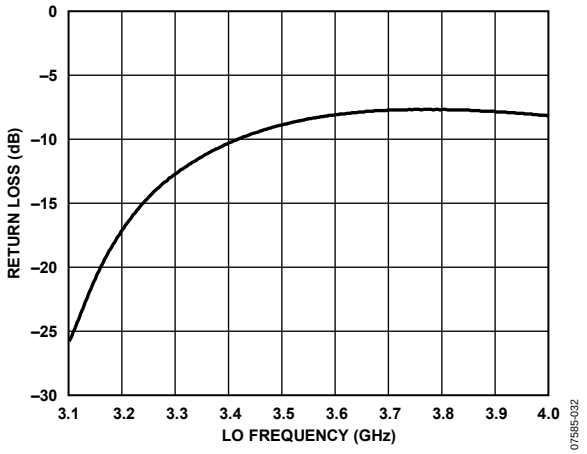


Figure 32. LO Port Return Loss vs. LO Frequency Measured on Characterization Board Through Johanson Technology 3600 Balun

HIGH BAND OPERATION

RF = 5 GHz to 6 GHz; Johanson Technology 5400BL15B050E balun on LO and RF inputs, the ADJ pin is open.

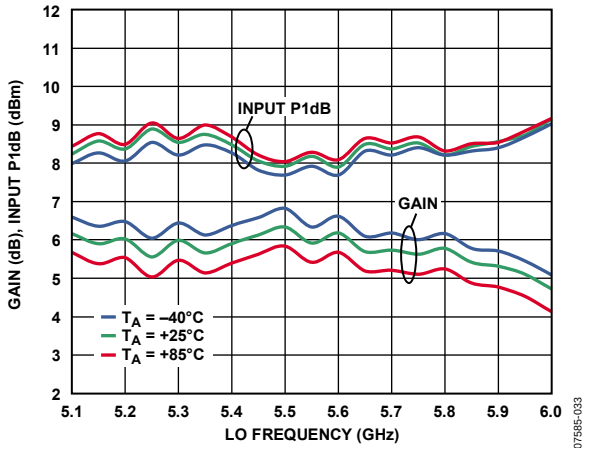


Figure 33. Conversion Gain and Input 1 dB Compression Point (IP1dB) vs. LO Frequency

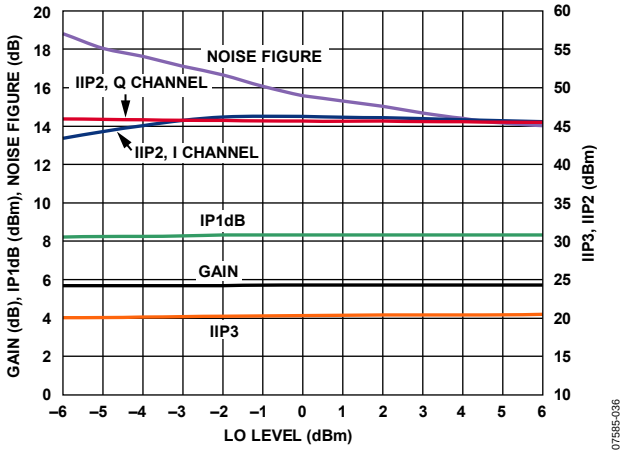


Figure 36. Conversion Gain, IP1dB, Noise Figure, IIP3, and IIP2 vs. LO Level, f_{LO} = 5800 MHz

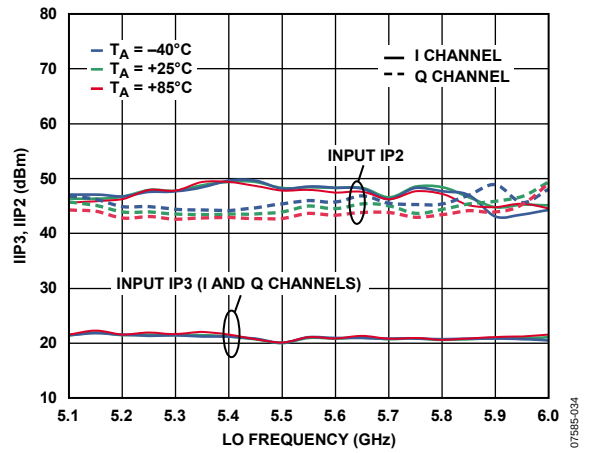


Figure 34. Input Third-Order Intercept (IIP3) and Input Second-Order Intercept Point (IIP2) vs. LO Frequency

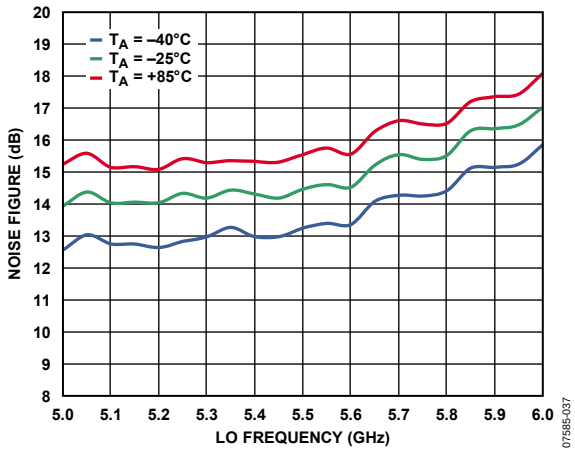


Figure 37. Noise Figure vs. LO Frequency

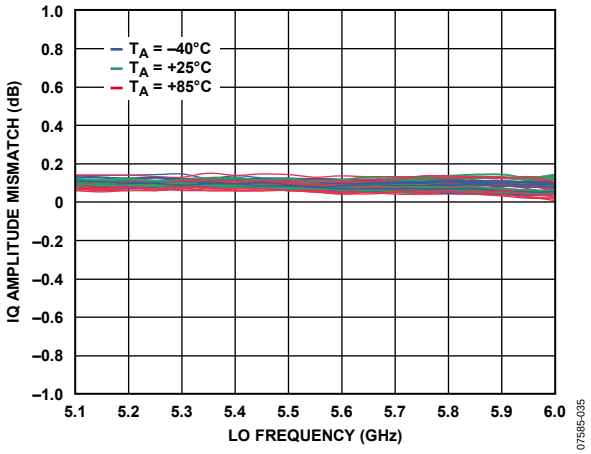


Figure 35. IQ Gain Mismatch vs. LO Frequency

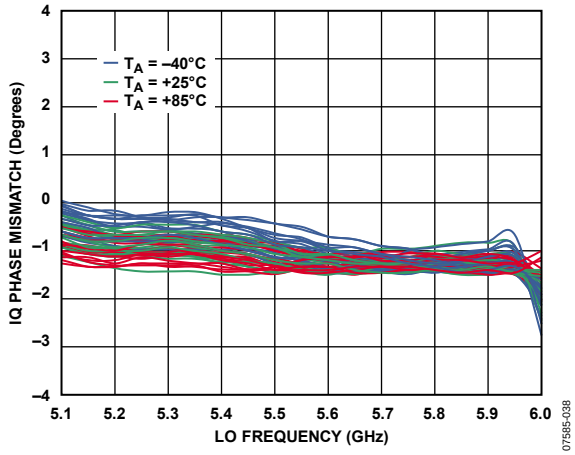


Figure 38. IQ Quadrature Phase Error vs. LO Frequency

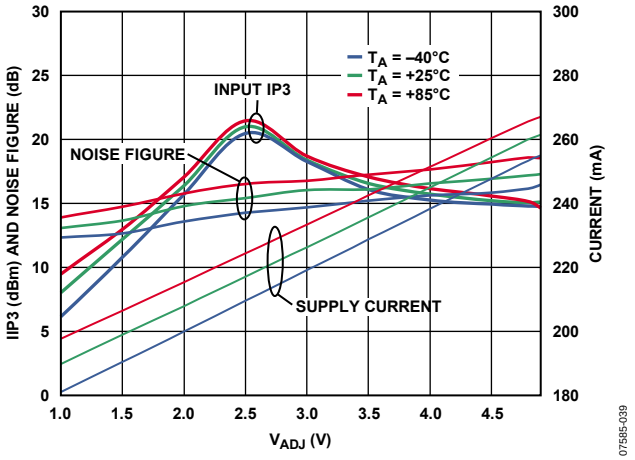


Figure 39. IIP3, Noise Figure, and Supply Current vs. V_{ADJ}, f_{LO} = 5800 MHz

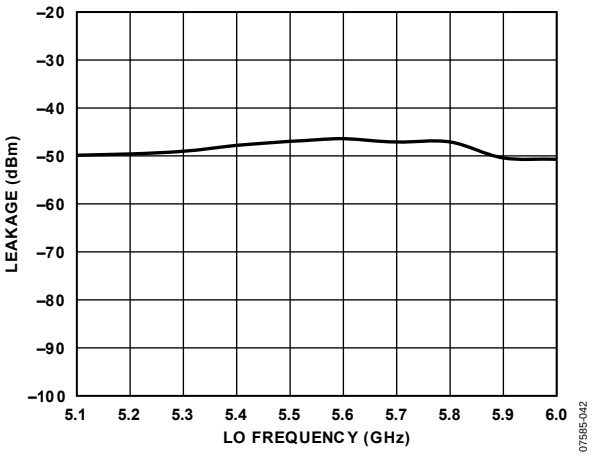


Figure 42. LO-to-RF Leakage vs. LO Frequency

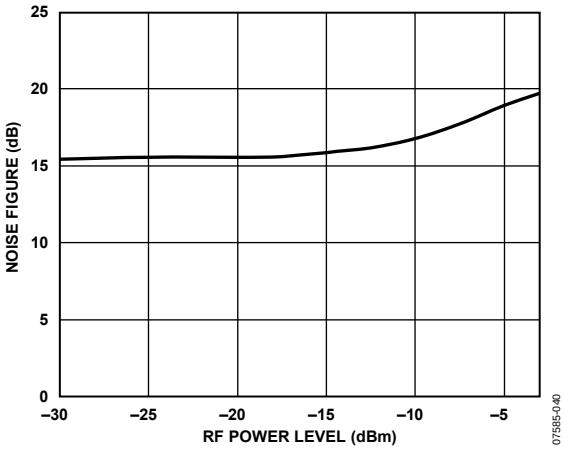


Figure 40. Noise Figure vs. Input Blocker Level, f_{LO} = 5800 MHz (RF Blocker 5 MHz Offset)

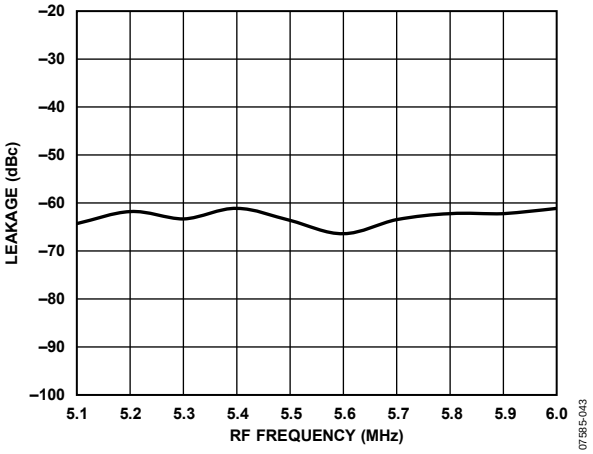


Figure 43. RF-to-LO Leakage vs. RF Frequency

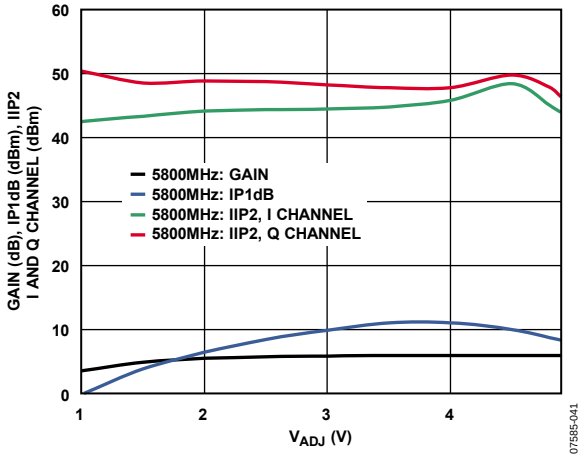


Figure 41. Conversion Gain, IP1dB, and IIP2 vs. R_{BIAS}, f_{LO} = 5800 MHz

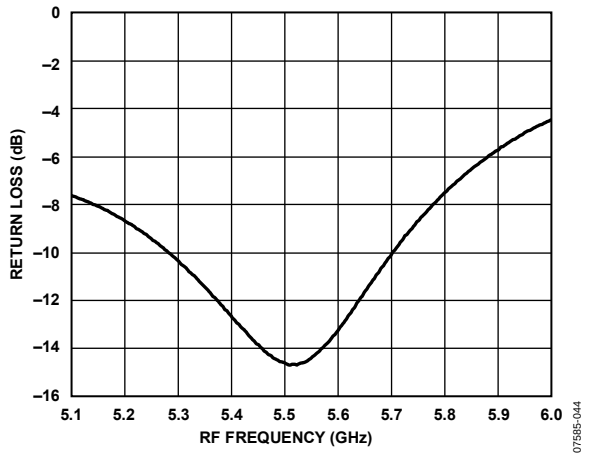


Figure 44. RF Port Return Loss vs. RF Frequency Measured on Characterization Board Through Johanson Technology 5400 Balun

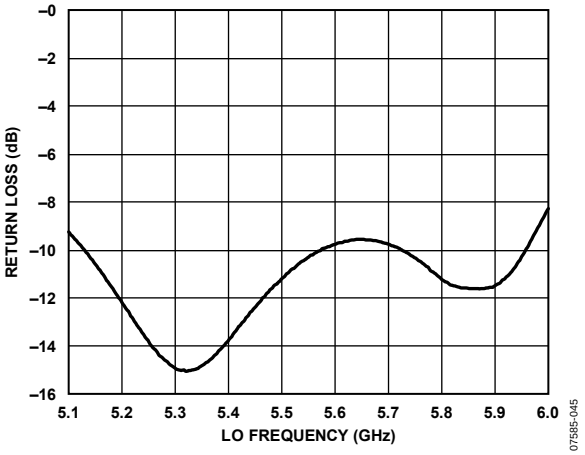


Figure 45. LO Port Return Loss vs. LO Frequency Measured on Characterization Board Through Johanson Technology 5400 Balun

DISTRIBUTIONS FOR f_{LO} = 900 MHz

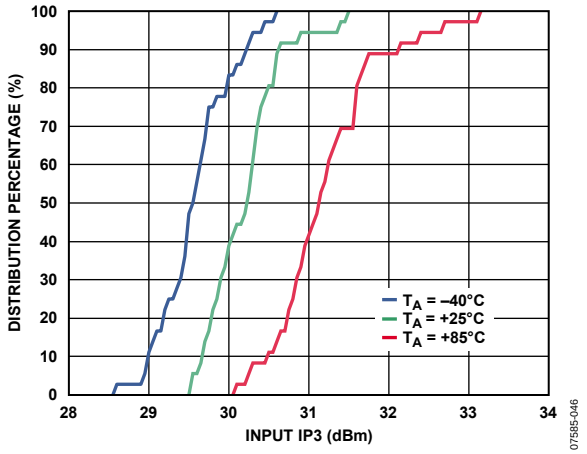


Figure 46. IIP3 Distributions

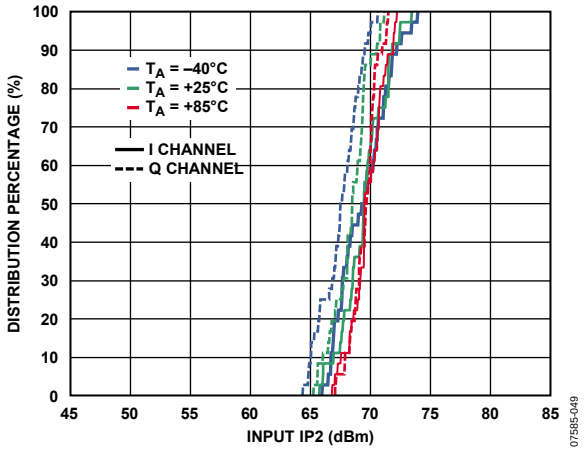


Figure 49. IIP2 Distributions for I Channel and Q Channel

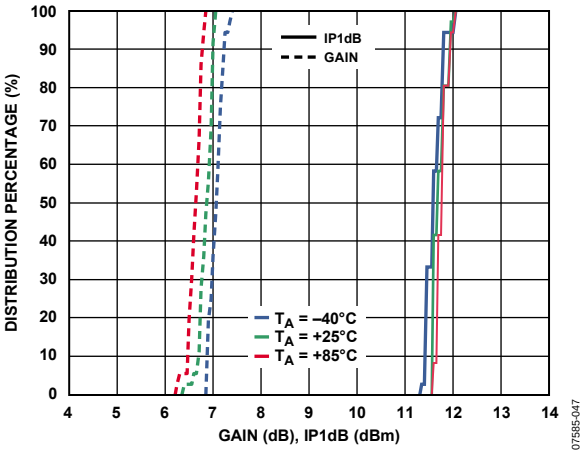


Figure 47. Gain and IP1dB Distributions

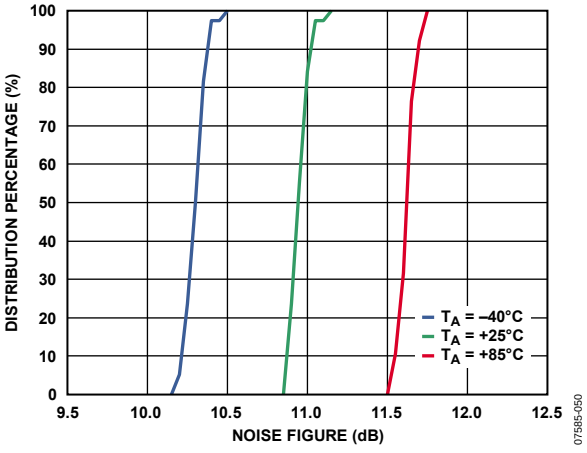


Figure 50. Noise Figure Distributions

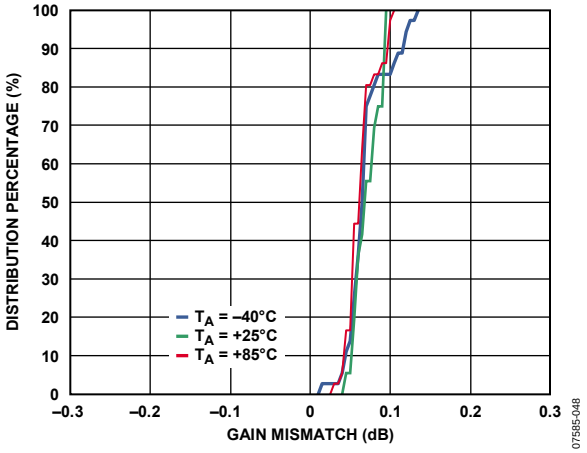


Figure 48. IQ Gain Mismatch Distributions

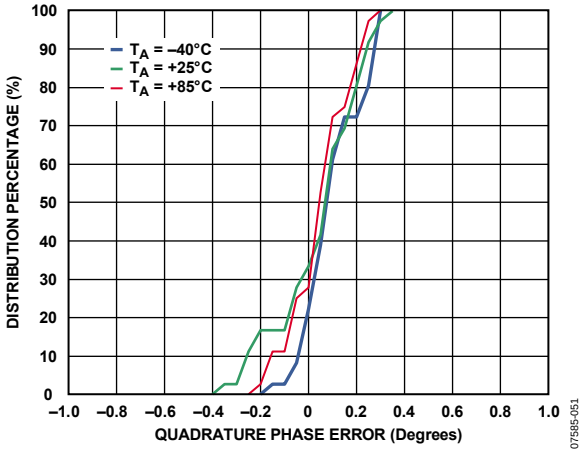


Figure 51. IQ Quadrature Phase Error Distributions

DISTRIBUTIONS FOR f_{LO} = 1900 MHz

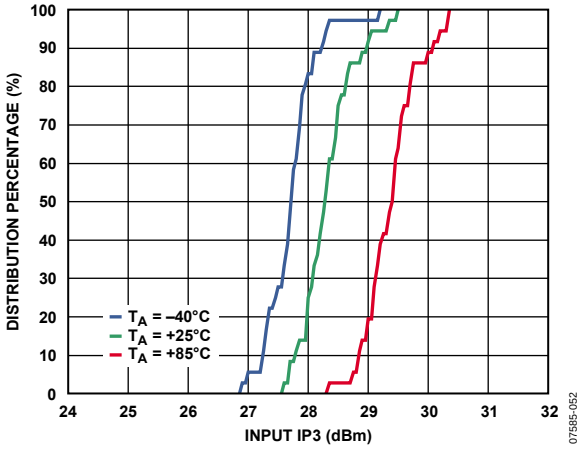


Figure 52. IIP3 Distributions

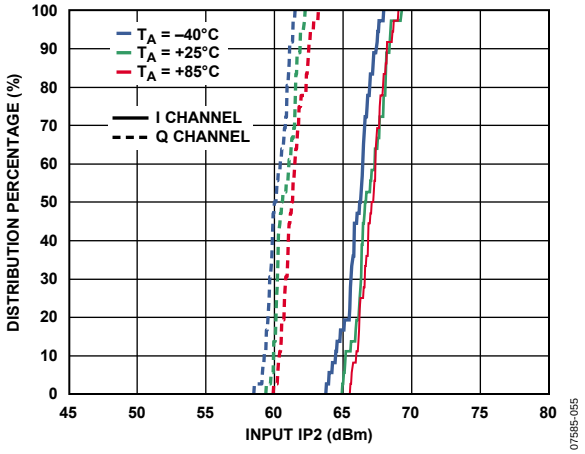


Figure 55. IIP2 Distributions for I Channel and Q Channel

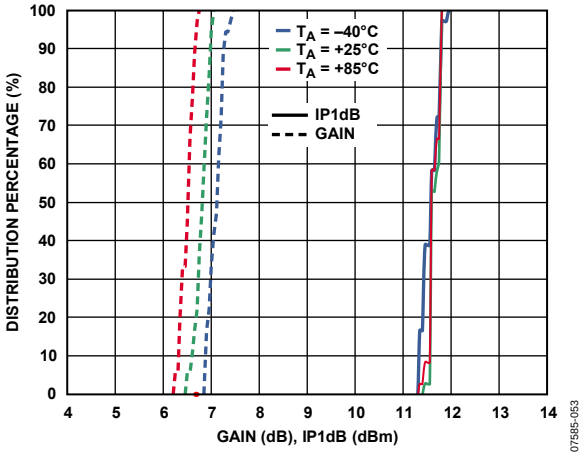


Figure 53. Gain and IP1dB Distributions

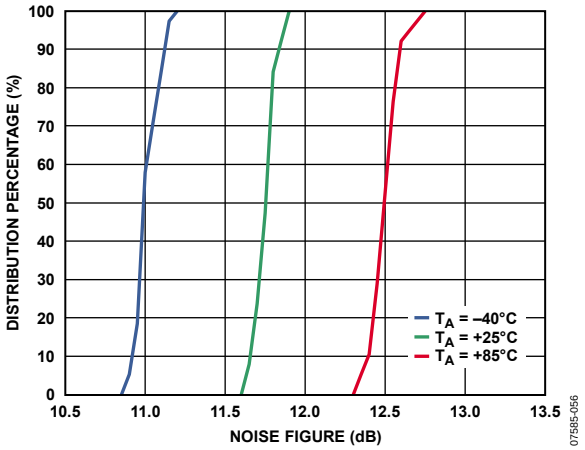


Figure 56. Noise Figure Distributions

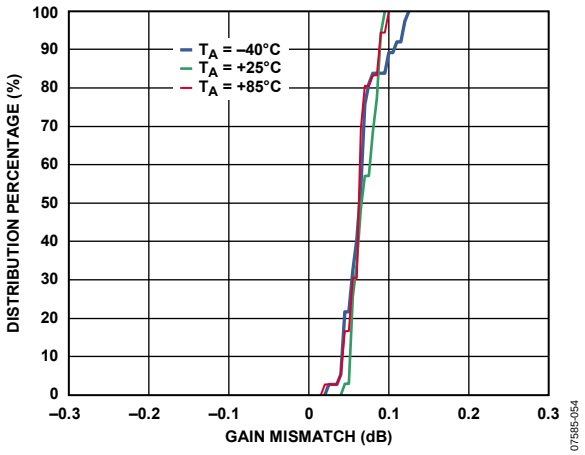


Figure 54. IQ Gain Mismatch Distributions

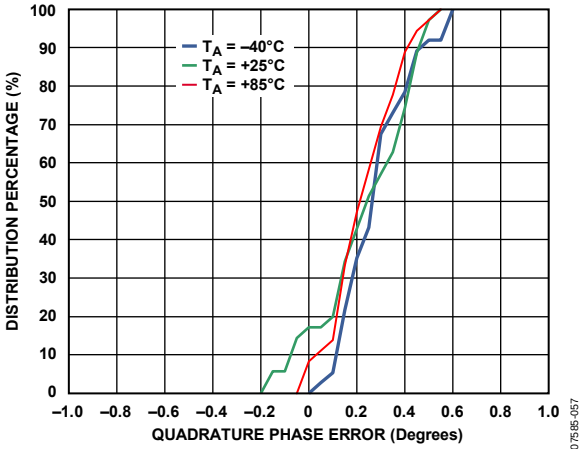


Figure 57. IQ Quadrature Phase Error Distributions

DISTRIBUTIONS FOR f_{LO} = 2700 MHz

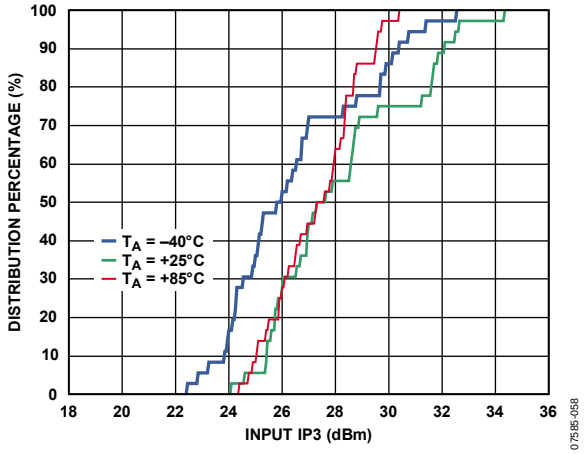


Figure 58. IIP3 Distributions

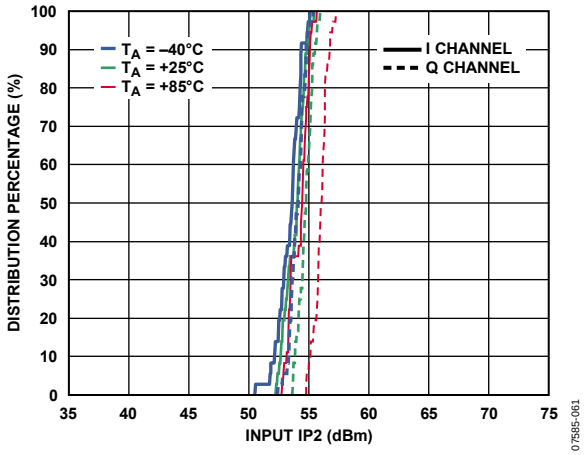


Figure 61. IIP2 Distributions for I Channel and Q Channel

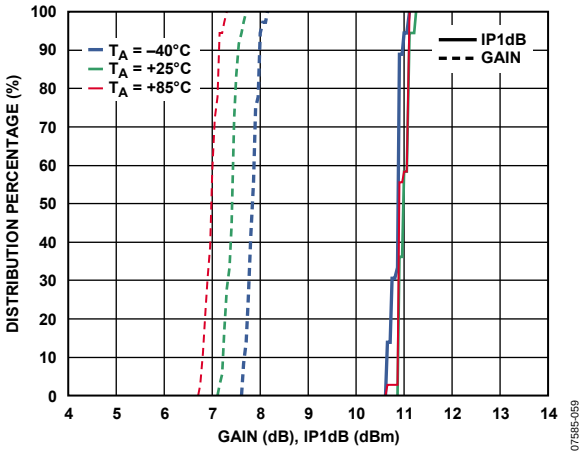


Figure 59. Gain and IP1dB Distributions

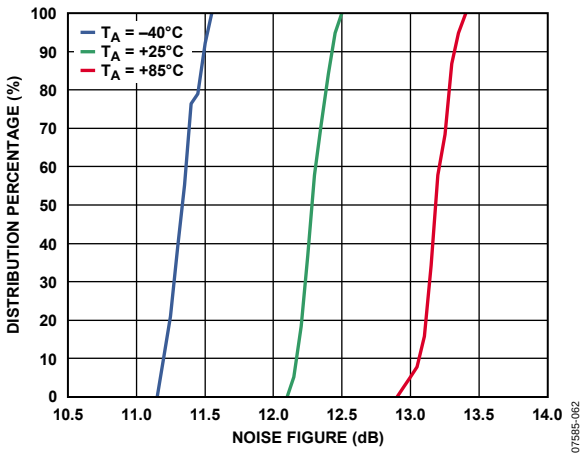


Figure 62. Noise Figure Distributions

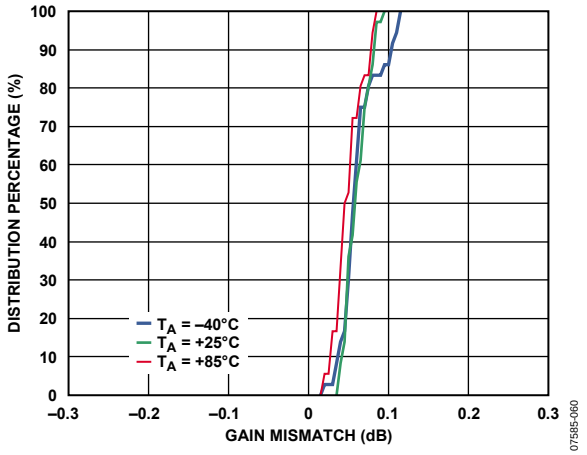


Figure 60. IQ Gain Mismatch Distributions

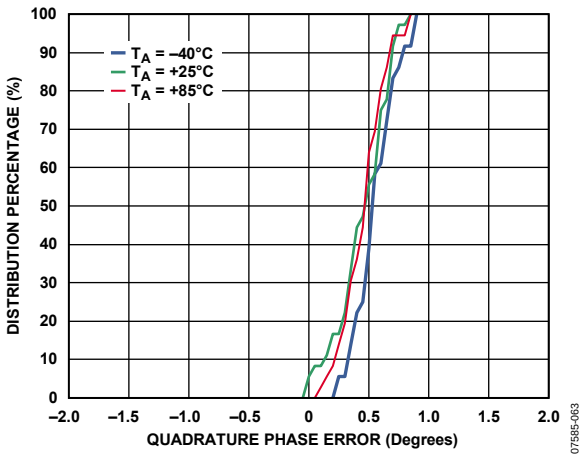


Figure 63. IQ Quadrature Phase Error Distributions

DISTRIBUTIONS FOR f_{LO} = 3600 MHz

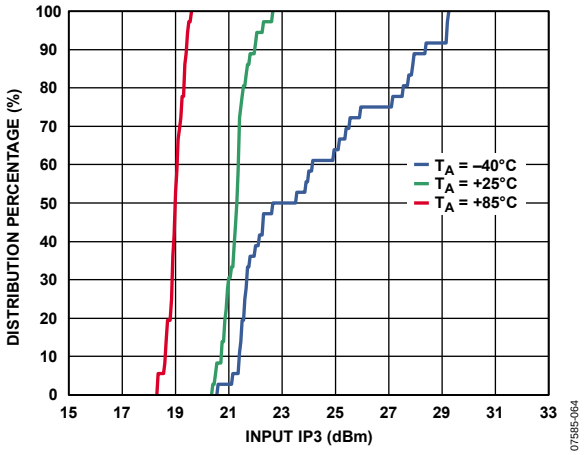


Figure 64. IIP3 Distributions

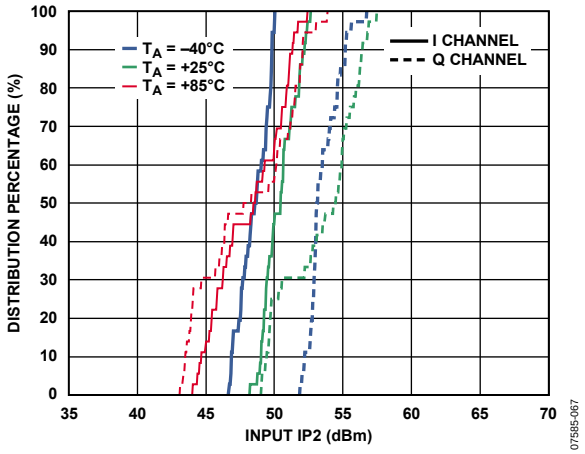


Figure 67. IIP2 Distributions for I Channel and Q Channel

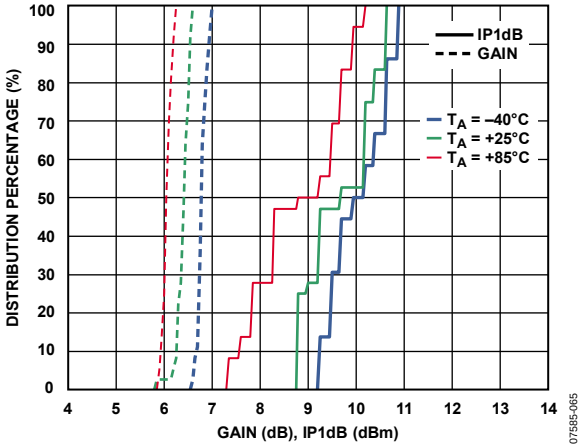


Figure 65. Gain and IP1dB Distributions

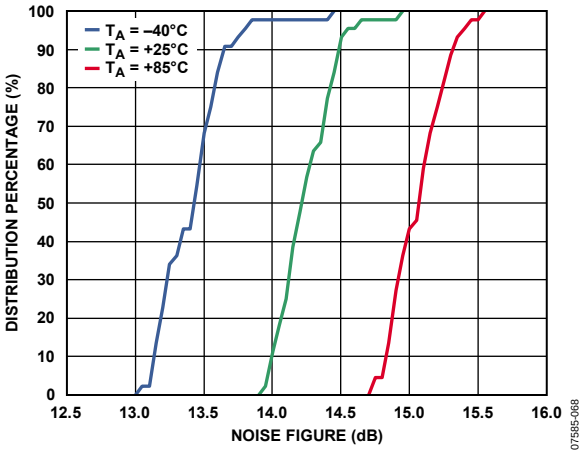


Figure 68. Noise Figure Distributions

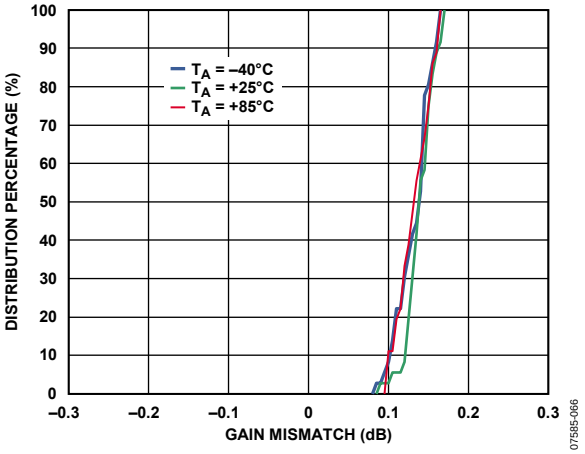


Figure 66. IQ Gain Mismatch Distributions

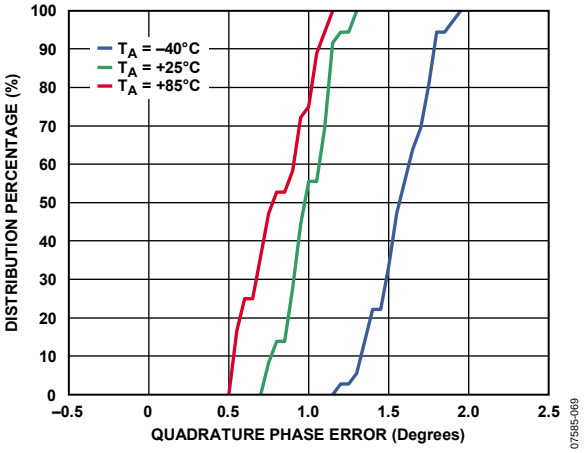


Figure 69. IQ Quadrature Phase Error Distributions

DISTRIBUTIONS FOR f_{LO} = 5800 MHz

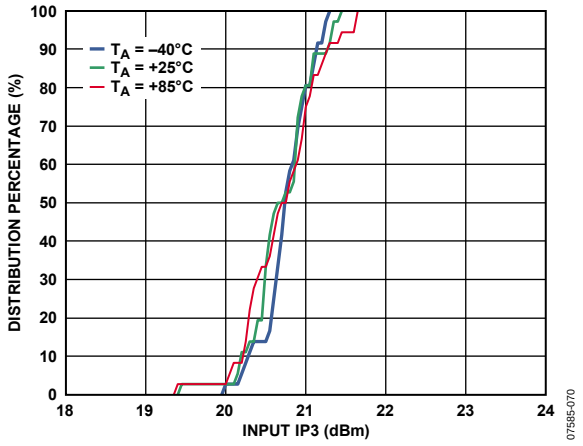


Figure 70. IIP3 Distributions

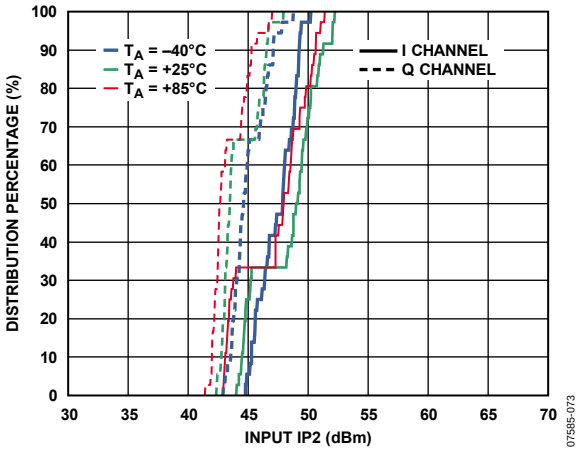


Figure 73. IIP2 Distributions for I Channel and Q Channel

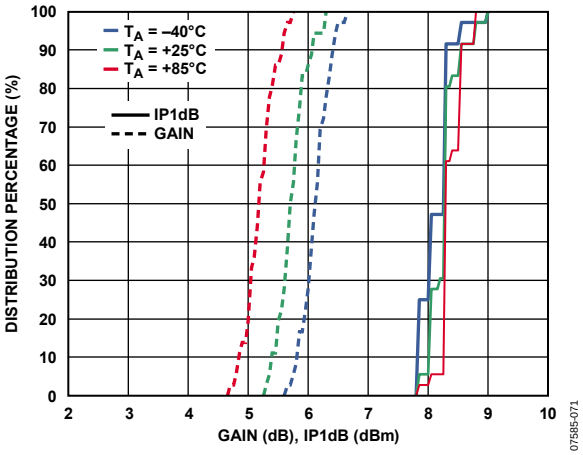


Figure 71. Gain and IP1dB Distributions

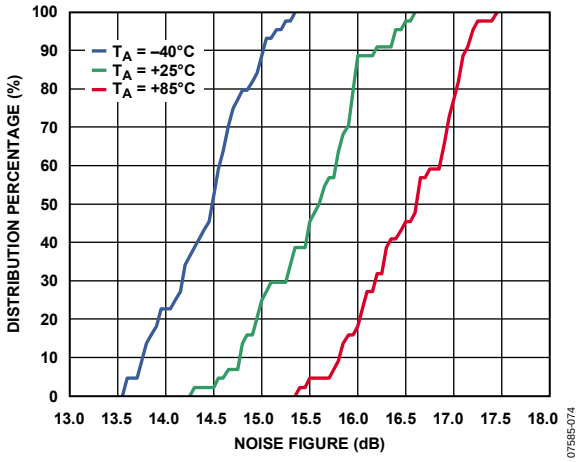


Figure 74. Noise Figure Distributions

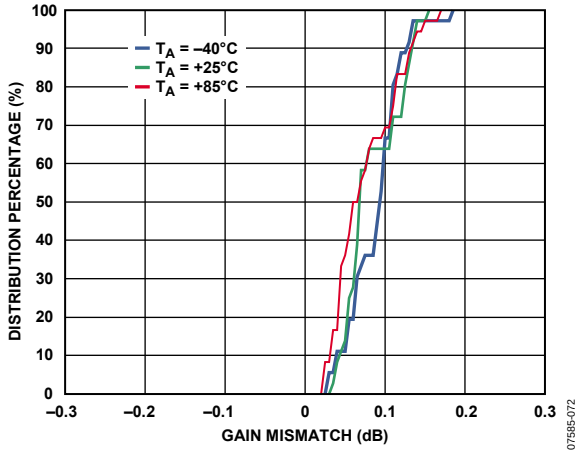


Figure 72. IQ Gain Mismatch Distributions

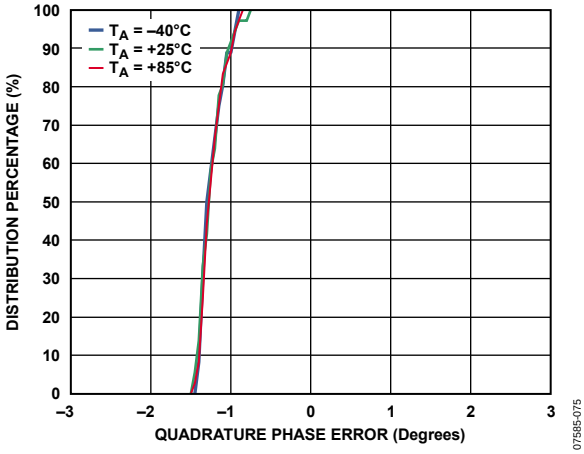


Figure 75. IQ Quadrature Phase Error Distributions

CIRCUIT DESCRIPTION

The ADL5380 can be divided into five sections: the local oscillator (LO) interface, the RF voltage-to-current (V-to-I) converter, the mixers, the differential emitter follower outputs, and the bias circuit. A detailed block diagram of the device is shown in Figure 76.

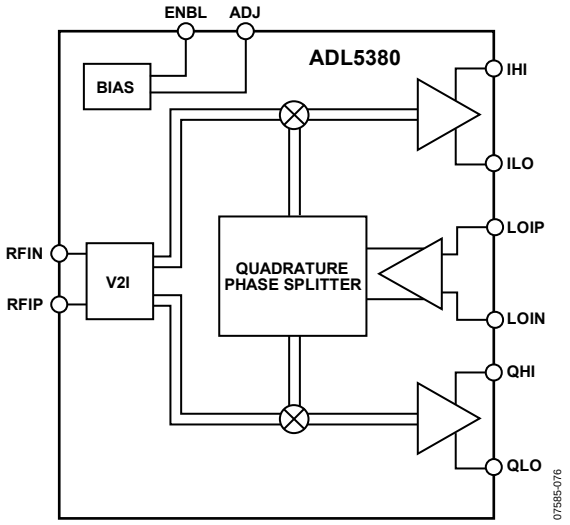


Figure 76. Block Diagram

The LO interface generates two LO signals at 90° of phase difference to drive two mixers in quadrature. RF signals are converted into currents by the V-to-I converters that feed into the two mixers. The differential I and Q outputs of the mixers are buffered via emitter followers. Reference currents to each section are generated by the bias circuit. A detailed description of each section follows.

LO INTERFACE

The LO interface consists of a polyphase quadrature splitter followed by a limiting amplifier. The LO input impedance is set by the polyphase, which splits the LO signal into two differential signals in quadrature. The LO input impedance is nominally 50 Ω. Each quadrature LO signal then passes through a limiting amplifier that provides the mixer with a limited drive signal. For optimal performance, the LO inputs must be driven differentially.

V-TO-I CONVERTER

The differential RF input signal is applied to a V-to-I converter that converts the differential input voltage to output currents. The V-to-I converter provides a differential 50 Ω input impedance. The V-to-I bias current can be adjusted up or down using the ADJ pin (Pin 19). Adjusting the current up improves IIP3 and IP1dB but degrades SSB NF. Adjusting the current down improves SSB NF but degrades IIP3 and IP1dB. The current adjustment can be made by connecting a resistor from the ADJ pin (Pin 19) to V_S to increase the bias current or to ground to decrease the bias current. Table 4 approximately dictates the relationship between the resistor used (R_{ADJ}), the resulting ADJ pin voltage, and the resulting baseband common-mode output voltage.

Table 4. ADJ Pin Resistor Values and Approximate ADJ Pin Voltages

R_{ADJ}	~V_{ADJ} (V)	~ Baseband Common-Mode Output (V)
200 Ω to V_S	4.8	2.2
600 Ω to V_S	4.5	2.3
1.54 kΩ to V_S	4	2.5
3.8 kΩ to V_S	3.5	2.7
10 kΩ to V_S	3	3
Open	2.5	3.2
9 kΩ to GND	2	3.4
3.5 kΩ to GND	1.5	3.6
1.5 kΩ to GND	1	3.8

MIXERS

The ADL5380 has two double-balanced mixers: one for the in-phase channel (I channel) and one for the quadrature channel (Q channel). These mixers are based on the Gilbert cell design of four cross-connected transistors. The output currents from the two mixers are summed together in the resistive loads that then feed into the subsequent emitter follower buffers.

EMITTER FOLLOWER BUFFERS

The output emitter followers drive the differential I and Q signals off chip. The output impedance is set by on-chip 25 Ω series resistors that yield a 50 Ω differential output impedance for each baseband port. The fixed output impedance forms a voltage divider with the load impedance that reduces the effective gain. For example, a 500 Ω differential load has 1 dB lower effective gain than a high (10 kΩ) differential load impedance.

BIAS CIRCUIT

A band gap reference circuit generates the reference currents used by different sections. The bias circuit can be enabled and partially disabled using ENBL (Pin 7). If ENBL is grounded or left open, the part is fully enabled. Pulling ENBL high shuts off certain sections of the bias circuitry, reducing the standing power to about half of its fully enabled consumption and disabling the outputs.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 78 shows the basic connections schematic for the ADL5380.

POWER SUPPLY

The nominal voltage supply for the ADL5380 is 5 V and is applied to the VCC1, VCC2, and VCC3 pins. Connect ground to the GND1, GND2, GND3, and GND4 pins. Solder the exposed paddle on the underside of the package to a low thermal and electrical impedance ground plane. If the ground plane spans multiple layers on the circuit board, these layers should be stitched together with nine vias under the exposed paddle. The AN-772 Application Note discusses the thermal and electrical grounding of the LFCSP in detail. Decouple each of the supply pins using two capacitors; recommended capacitor values are 100 pF and 0.1 µF.

LOCAL OSCILLATOR (LO) INPUT

For optimum performance, drive the LO port differentially through a balun. The recommended balun for each performance level includes the following:

- Up to 3 GHz is the Mini-Circuits TC1-1-13.
- From 3 GHz to 4 GHz is the Johanson Technology 3600BL14M050.
- From 4.9 GHz to 6 GHz is the Johanson Technology 5400BL15B050.

AC couple the LO inputs to the device with 100 pF capacitors. The LO port is designed for a broadband 50 Ω match from 400 MHz to 6 GHz. The LO return loss can be seen in Figure 19. Figure 77 shows the LO input configuration.

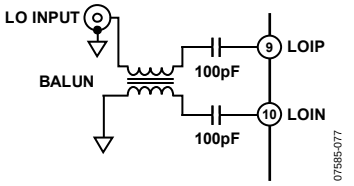


Figure 77. Differential LO Drive

The recommended LO drive level is between −6 dBm and +6 dBm. The applied LO frequency range is between 400 MHz and 6 GHz.

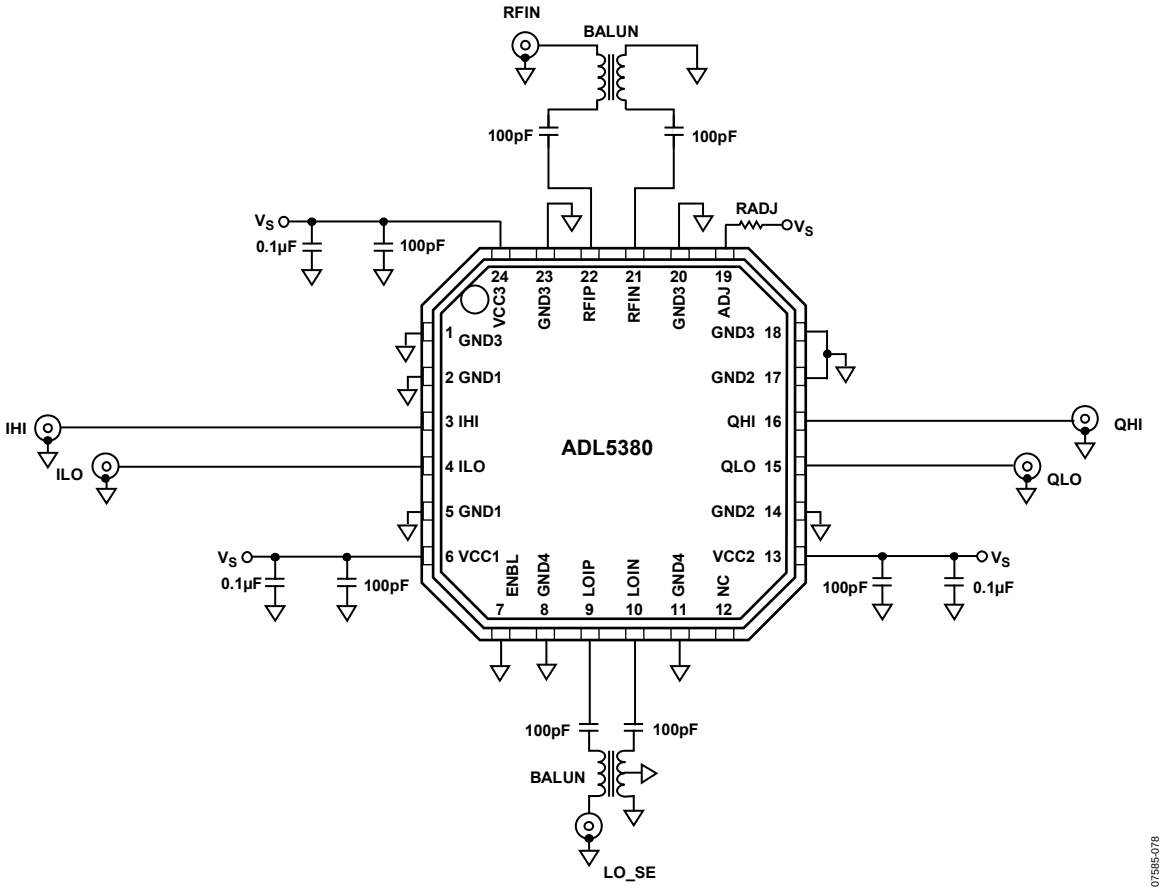


Figure 78. Basic Connections Schematic

RF INPUT

The RF inputs have a differential input impedance of approximately 50 Ω. For optimum performance, drive the RF port differentially through a balun. The recommended balun for each performance level includes the following:

- Up to 3 GHz is the Mini-Circuits TC1-1-13.
- From 3 GHz to 4 GHz is the Johanson Technology 3600BL14M050.
- From 4.9 GHz to 6 GHz is the Johanson Technology 5400BL15B050.

AC couple the RF inputs to the device with 100 pF capacitors. Figure 79 shows the RF input configuration.

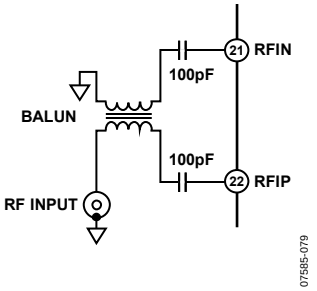


Figure 79. RF Input

The differential RF port return loss is characterized, as shown in Figure 80.

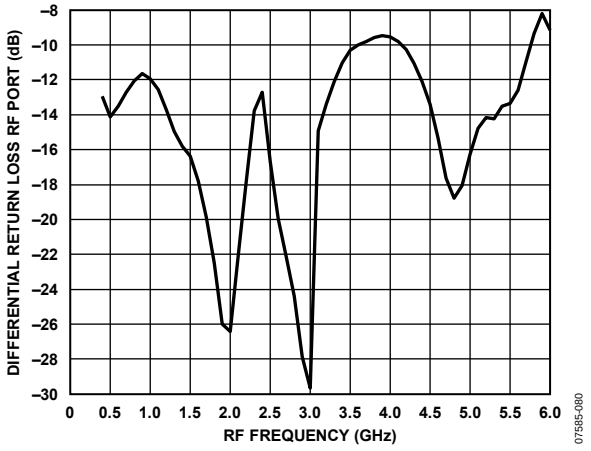


Figure 80. Differential RF Port Return Loss

BASEBAND OUTPUTS

The baseband outputs QHI, QLO, IHI, and ILO are fixed impedance ports. Each baseband pair has a 50 Ω differential output impedance. The outputs can be presented with differential loads as low as 200 Ω (with some degradation in gain) or high impedance differential loads (500 Ω or greater impedance yields the same excellent linearity) that is typical of an ADC. The TCM9-1 9:1 balun converts the differential IF output to a single-ended output. When loaded with 50 Ω, this balun presents a 450 Ω load to the device. The typical maximum linear voltage swing for these outputs is 2 V p-p differential. The output 3 dB bandwidth is 390 MHz. Figure 81 shows the baseband output configuration.

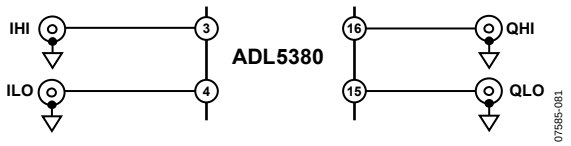


Figure 81. Baseband Output Configuration

ERROR VECTOR MAGNITUDE (EVM) PERFORMANCE

EVM is a measure used to quantify the performance of a digital radio transmitter or receiver. A signal received by a receiver has all constellation points at their ideal locations; however, various imperfections in the implementation (such as magnitude imbalance, noise floor, and phase imbalance) cause the actual constellation points to deviate from their ideal locations.

In general, a demodulator exhibits three distinct EVM limitations vs. received input signal power. At strong signal levels, the distortion components falling in-band due to non-linearities in the device cause strong degradation to EVM as signal levels increase. At medium signal levels, where the demodulator behaves in a linear manner and the signal is well above any notable noise contributions, the EVM has a tendency to reach an optimum level determined dominantly by the quadrature accuracy of the demodulator and the precision of the test equipment. As signal levels decrease, such that noise is a major contribution, the EVM performance vs. the signal level exhibits a decibel-for-decibel degradation with decreasing signal level. At lower signal levels, where noise proves to be the dominant limitation, the decibel EVM proves to be directly proportional to the SNR.

The ADL5380 shows excellent EVM performance for various modulation schemes. Figure 82 shows the EVM performance of the ADL5380 with a 16 QAM, 200 kHz low IF.

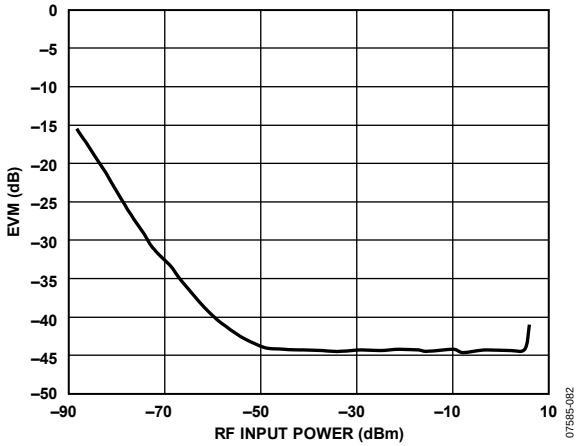


Figure 82. EVM, RF = 900 MHz, IF = 200 kHz vs. RF Input Power for a 16 QAM 160ksym/s Signal

Figure 83 shows the zero-IF EVM performance of a 10 MHz IEEE 802.16e WiMAX signal through the ADL5380. The differential dc offsets on the ADL5380 are in the order of a few millivolts. However, ac coupling the baseband outputs with 10 µF capacitors eliminates dc offsets and enhances EVM performance. With a 10 MHz BW signal, 10 µF ac coupling capacitors with the 500 Ω differential load results in a high-pass corner frequency of ~64 Hz, which absorbs an insignificant amount of modulated signal energy from the baseband signal. By using ac coupling capacitors at the baseband outputs, the dc offset effects, which can limit dynamic range at low input power levels, can be eliminated.

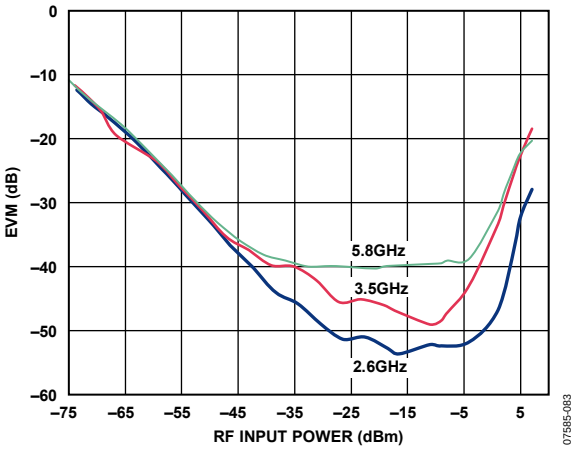


Figure 83. EVM, RF = 2.6 GHz, RF = 3.5 GHz, and RF = 5.8 GHz, IF = 0 Hz vs. RF Input Power for a 16 QAM 10 MHz Bandwidth Mobile WiMAX Signal (AC-Coupled Baseband Outputs)

Figure 84 exhibits multiple W-CDMA low-IF EVM performance curves over a wide RF input power range into the ADL5380. In the case of zero-IF, the noise contribution by the vector signal analyzer becomes predominant at lower power levels, making it difficult to measure SNR accurately.

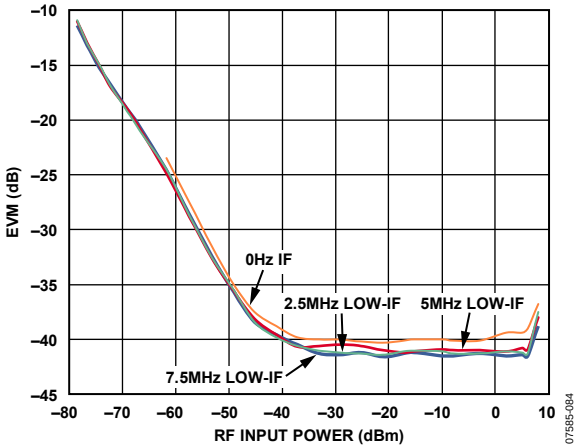


Figure 84. EVM, RF = 1900 MHz, IF = 0 Hz, IF = 2.5 MHz, IF = 5 MHz, and IF = 7.5 MHz vs. RF Input Power for a W-CDMA Signal (AC-Coupled Baseband Outputs)

LOW IF IMAGE REJECTION

The image rejection ratio is the ratio of the intermediate frequency (IF) signal level produced by the desired input frequency to that produced by the image frequency. The image rejection ratio is expressed in decibels. Appropriate image rejection is critical because the image power can be much higher than that of the desired signal, thereby plaguing the down-conversion process. Figure 85 illustrates the image problem. If the upper sideband (lower sideband) is the desired band, a 90° shift to the Q channel (I channel) cancels the image at the lower sideband (upper sideband). Phase and gain balance between I and Q channels are critical for high levels of image rejection.

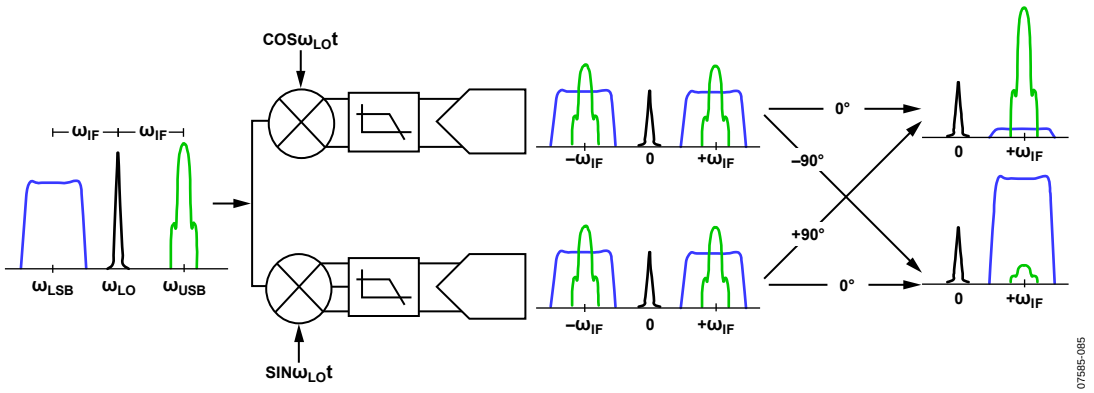


Figure 85. Illustration of the Image Problem

Figure 86 and Figure 87 show the excellent image rejection capabilities of the ADL5380 for low IF applications, such as W-CDMA. The ADL5380 exhibits image rejection greater than 45 dB over a broad frequency range.

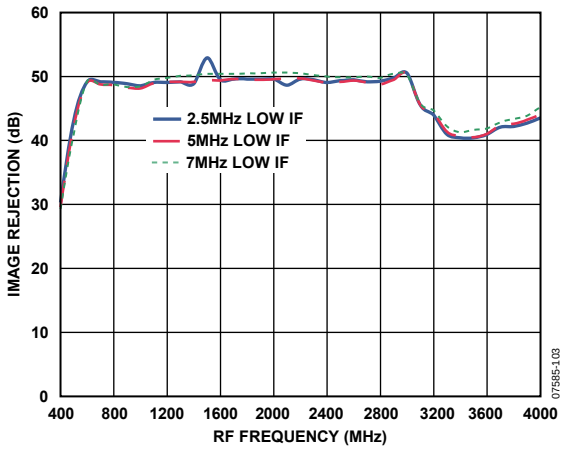


Figure 86. Low Band and Midband Image Rejection vs. RF Frequency for a W-CDMA Signal, IF = 2.5 MHz, 5 MHz, and 7.5 MHz

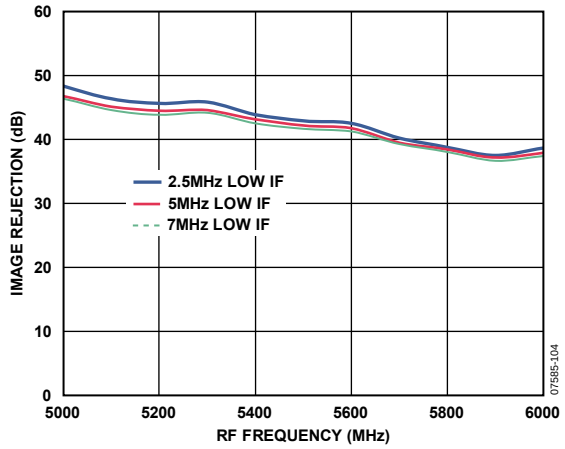


Figure 87. High Band Image Rejection vs. RF Frequency for a W-CDMA Signal, IF = 2.5 MHz, 5 MHz, and 7.5 MHz

EXAMPLE BASEBAND INTERFACE

In most direct-conversion receiver designs, it is desirable to select a wanted carrier within a specified band. The desired channel can be demodulated by tuning the LO to the appropriate carrier frequency. If the desired RF band contains multiple carriers of interest, the adjacent carriers are also down converted to a lower IF frequency. These adjacent carriers can be problematic if they are large relative to the wanted carrier because they can overdrive the baseband signal detection circuitry. As a result, it is often necessary to insert a filter to provide sufficient rejection of the adjacent carriers.

It is necessary to consider the overall source and load impedance presented by the ADL5380 and ADC input when designing the filter network. The differential baseband output impedance of the ADL5380 is 50 Ω. The ADL5380 is designed to drive a high impedance ADC input. It may be desirable to terminate the ADC input down to lower impedance by using a terminating resistor, such as 500 Ω. The terminating resistor helps to better define the input impedance at the ADC input at the cost of a slightly reduced gain (see the Circuit Description section for details on the emitter-follower output loading effects).

The order and type of filter network depends on the desired high frequency rejection required, pass-band ripple, and group delay. Filter design tables provide outlines for various filter types and orders, illustrating the normalized inductor and capacitor values for a 1 Hz cutoff frequency and 1 Ω load. After scaling the normalized prototype element values by the actual desired cut-off frequency and load impedance, the series reactance elements are halved to realize the final balanced filter network component values.

As an example, a second-order Butterworth, low-pass filter design is shown in Figure 88 where the differential load impedance is 500 Ω and the source impedance of the ADL5380 is 50 Ω. The normalized series inductor value for the 10-to-1, load-to-source impedance ratio is 0.074 H, and the normalized shunt capacitor is 14.814 F. For a 10.9 MHz cutoff frequency, the single-ended equivalent circuit consists of a 0.54 µH series inductor followed by a 433 pF shunt capacitor.

The balanced configuration is realized as the 0.54 µH inductor is split in half to realize the network shown in Figure 88.

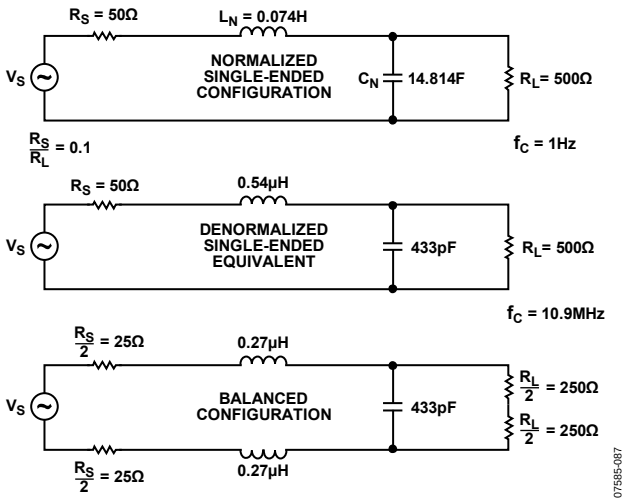


Figure 88. Second-Order Butterworth, Low-Pass Filter Design Example

A complete design example is shown in Figure 91. A sixth-order Butterworth differential filter having a 1.9 MHz corner frequency interfaces the output of the ADL5380 to that of an ADC input. The 500 Ω load resistor defines the input impedance of the ADC. The filter adheres to typical direct conversion W-CDMA applications where, 1.92 MHz away from the carrier IF frequency, 1 dB of rejection is desired, and, 2.7 MHz away from the carrier IF frequency, 10 dB of rejection is desired.

Figure 89 and Figure 90 show the measured frequency response and group delay of the filter.

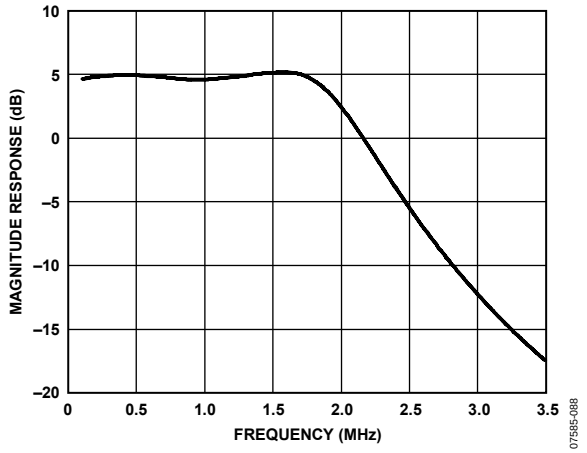


Figure 89. Sixth-Order Baseband Filter Response

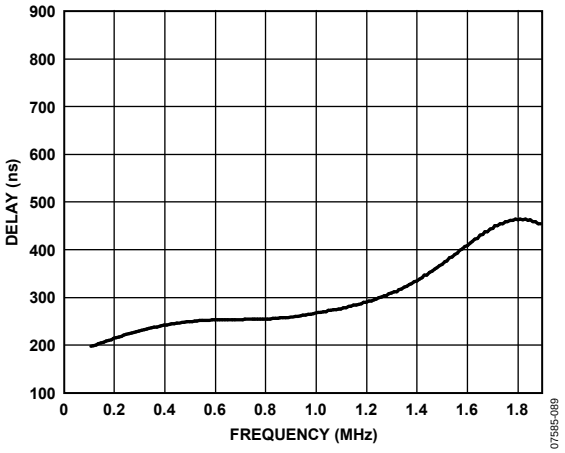


Figure 90. Sixth-Order Baseband Filter Group Delay

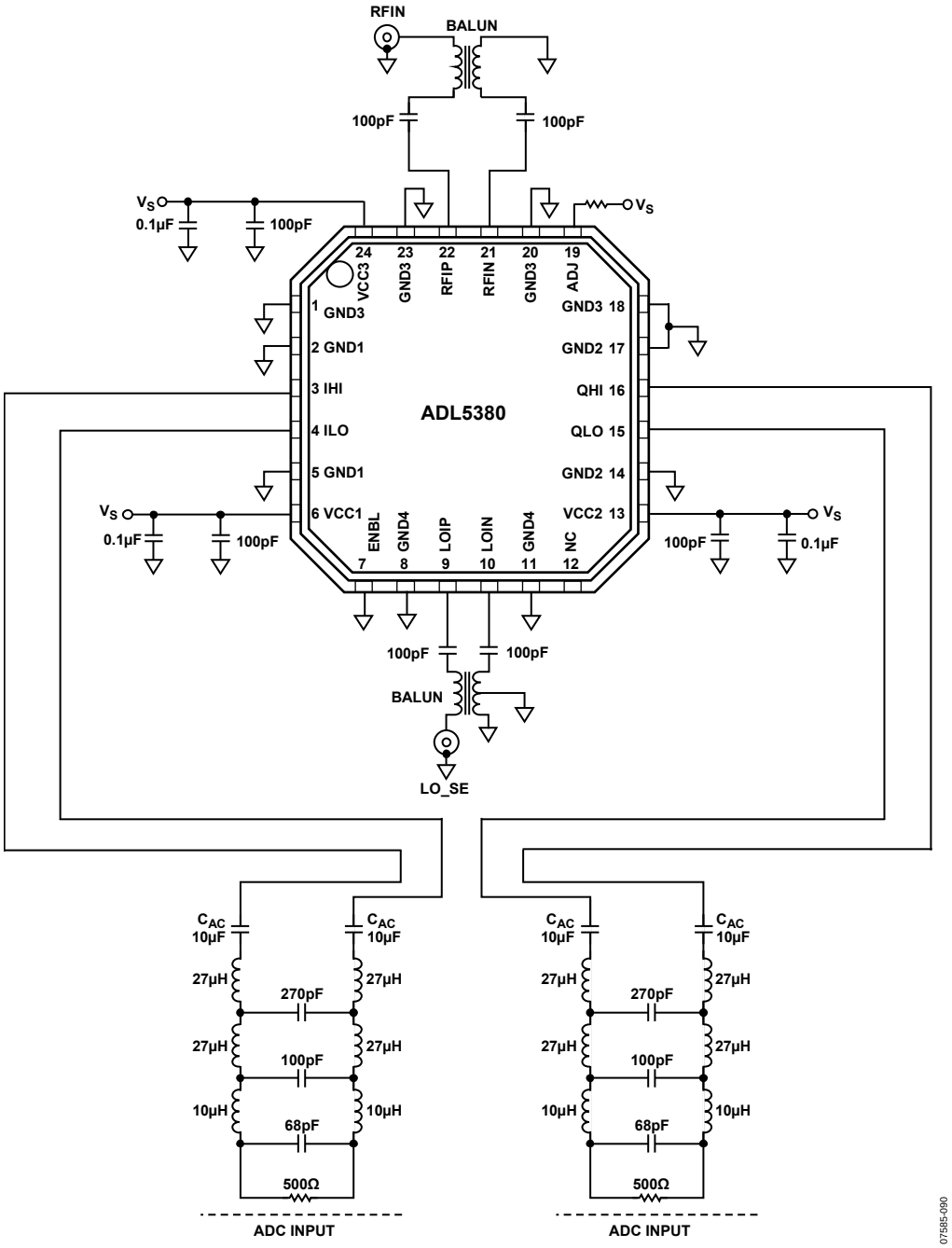


Figure 91. Sixth-Order Low-Pass Butterworth, Baseband Filter Schematic

As the load impedance of the filter increases, the filter design becomes more challenging in terms of meeting the required rejection and pass band specifications. In the previous W-CDMA example, the 500 Ω load impedance resulted in the design of a sixth-order filter that has relatively large inductor values and small capacitor values. If the load impedance is 200 Ω, the filter design becomes much more manageable. Figure 92 shows a fourth-order filter designed for a 10 MHz wide LTE signal. As shown in Figure 92, the resultant inductor and capacitor values become much more practical with a 200 Ω load.

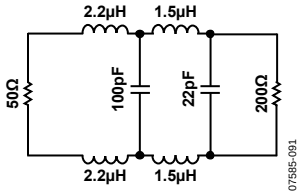


Figure 92. Fourth-Order Low-Pass LTE Filter Schematic

Figure 93 and Figure 94 illustrate the magnitude response and group delay response of the fourth-order filter, respectively.

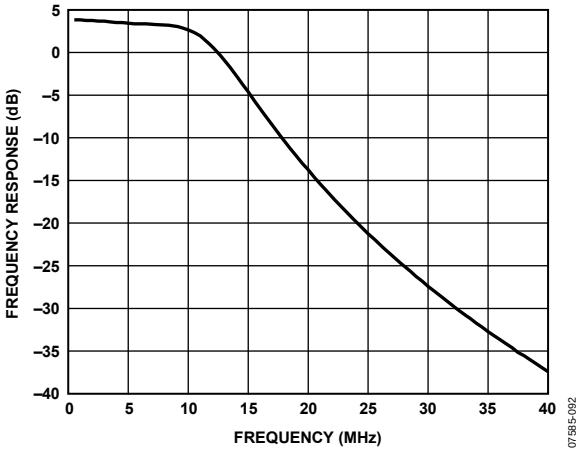


Figure 93. Fourth-Order Low-Pass LTE Filter Magnitude Response

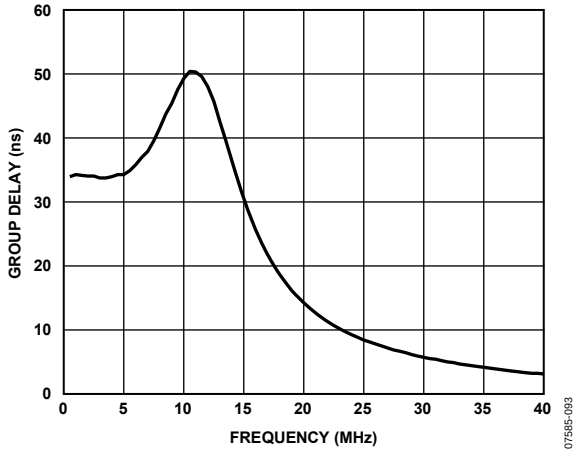


Figure 94. Fourth-Order Low-Pass LTE Filter Group Delay Response

CHARACTERIZATION SETUPS

Figure 95 to Figure 97 show the general characterization bench setups used extensively for the ADL5380. The setup shown in Figure 97 was used to do the bulk of the testing and used sinusoidal signals on both the LO and RF inputs. An automated Agilent VEE program was used to control the equipment over the IEEE bus. This setup was used to measure gain, IP1dB, IIP2, IIP3, I/Q gain match, and quadrature error. The ADL5380 characterization board had a 9-to-1 impedance transformer on each of the differential baseband ports to do the differential-to-single-ended conversion, which presented a 450 Ω differential load to each baseband port, when interfaced with 50 Ω test equipment.

For all measurements of the ADL5380, the loss of the RF input balun was de-embedded. Due to the wideband nature of the ADL5380, three different board configurations had to be used to characterize the product. For low band characterization (400 MHz to 3 GHz), the Mini-Circuits TC1-1-13 balun was used on the RF and LO inputs to create differential signals at the device pins. For midband characterization (3 GHz to 4 GHz), the Johanson Technology 3600BL14M050T was used, and for high band characterization (5 GHz to 6 GHz), the Johanson Technology 5400BL15B050E balun was used.

The two setups shown in Figure 95 and Figure 96 were used for making NF measurements. Figure 95 shows the setup for measuring NF with no blocker signal applied while Figure 96 was used to measure NF in the presence of a blocker. For both setups, the noise was measured at a baseband frequency of 10 MHz. For the case where a blocker was applied, the output blocker was at a 15 MHz baseband frequency. Note that great care must be taken when measuring NF in the presence of a blocker. The RF blocker generator must be filtered to prevent its noise (which increases with increasing generator output power) from swamping the noise contribution of the ADL5380. At least 30 dB of attention at the RF and image frequencies is desired. For example, assume a 915 MHz signal applied to the LO inputs of the ADL5380. To obtain a 15 MHz output blocker signal, the RF blocker generator is set to 930 MHz and the filters tuned such that there is at least 30 dB of attenuation from the generator at both the desired RF frequency (925 MHz) and the image RF frequency (905 MHz). Finally, the blocker must be removed from the output (by the 10 MHz low-pass filter) to prevent the blocker from swamping the analyzer.

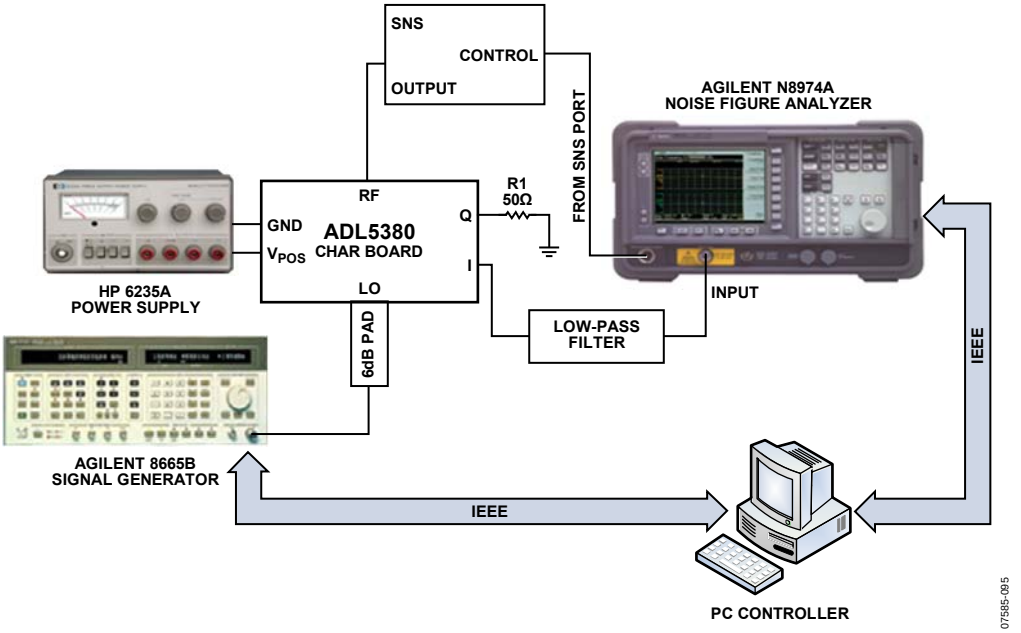


Figure 95. General Noise Figure Measurement Setup

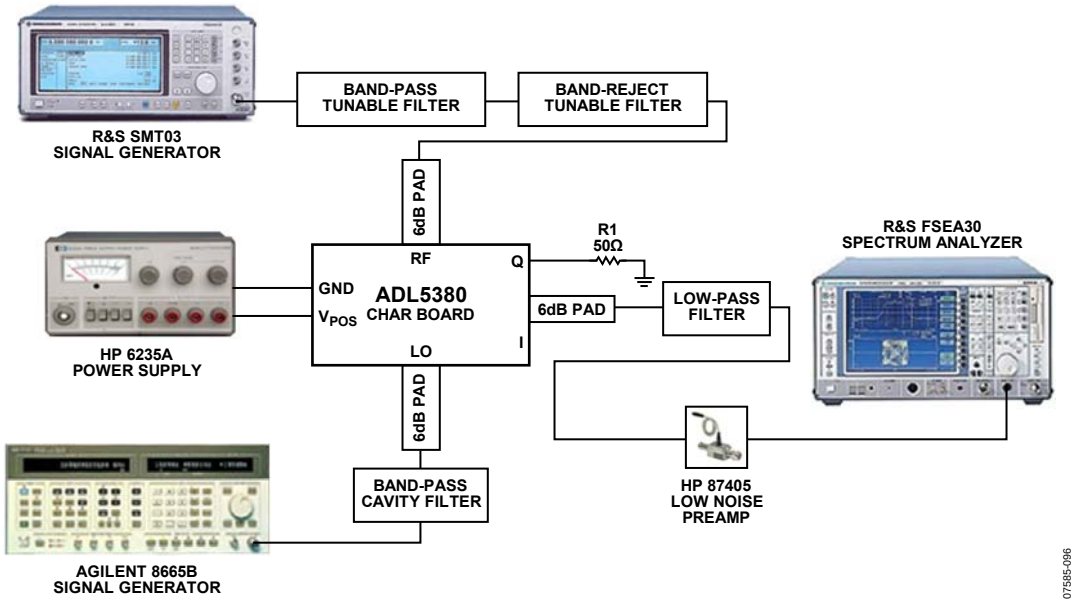


Figure 96. Measurement Setup for Noise Figure in the Presence of a Blocker

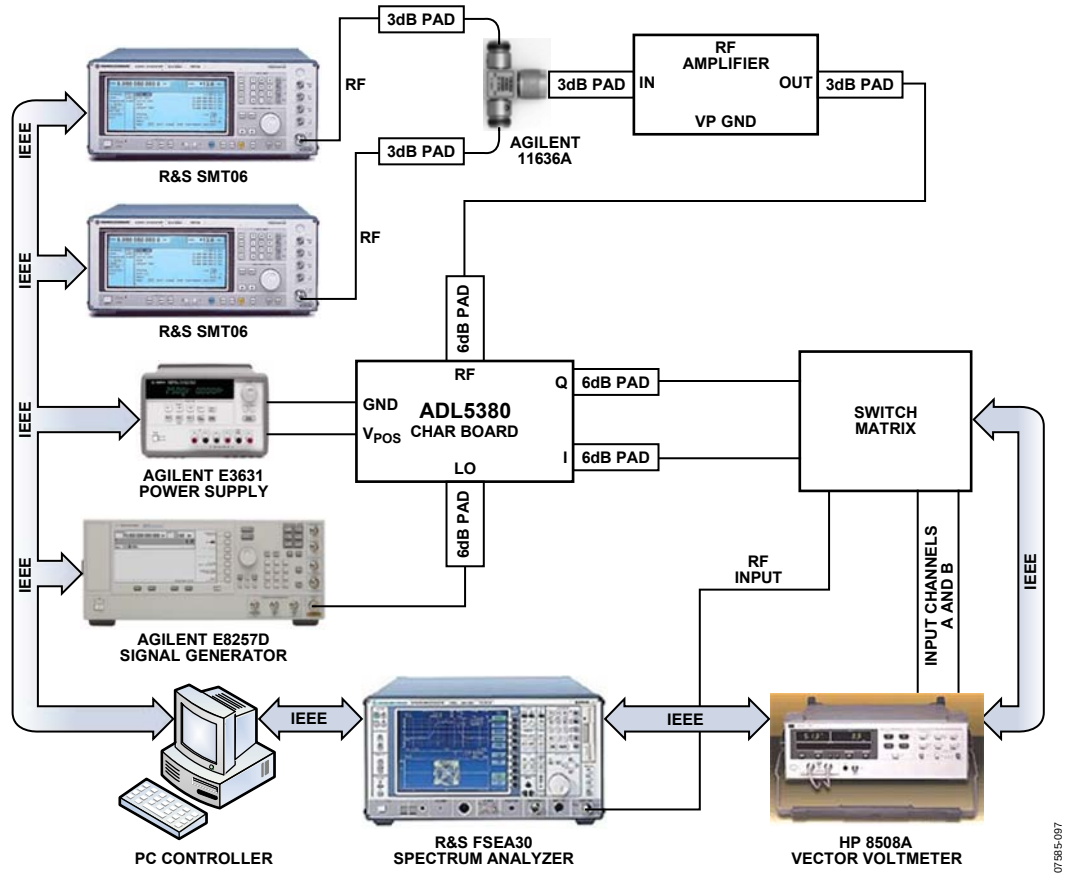


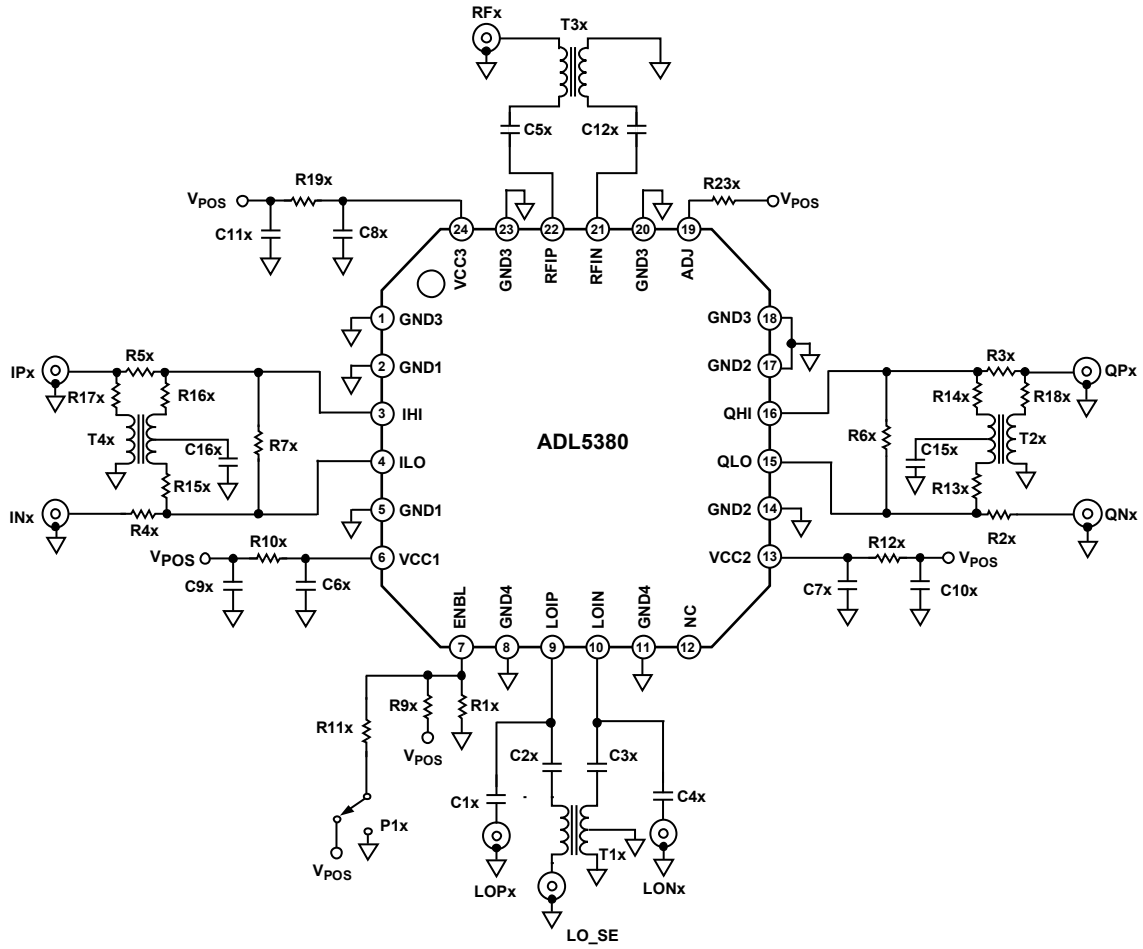
Figure 97. General Characterization Setup

EVALUATION BOARD

The ADL5380 evaluation board is available. There are two versions of the board, optimized for performance for separate frequency ranges. For operation <3 GHz, an FR4 material-based board with the TC1-1-13 balun footprint is available. For operation between 3 GHz to 6 GHz, a Rogers® material-based RO3003 board with the Johanson Technology 3600BL14M050 balun (optimal for operation between 3 GHz and 4 GHz) footprint is available.

The Johanson Technology 5400BL15K050 shares the same footprint and can be used for operation between 4900 MHz to 5800 MHz.

The board can be used for single-ended or differential baseband analysis. The default configuration of the board is for single-ended baseband analysis.



NOTES
1. X = B, FOR LOW FREQUENCY OPERATION UP TO 3GHz, TC1-1-13 BALUN ON RF AND LO PORTS.
X = A, FOR FREQUENCY OPERATION FROM 3GHz TO 4GHz, JOHANSON TECHNOLOGY 3600BL14M050 BALUN ON RF AND LO PORTS.

2. FOR OPERATION BETWEEN 4.9GHZ TO 6GHZ, THE JOHANSON TECHNOLOGY 5400BL15K050 BALUN, WHICH SHARES A SIMILAR FOOTPRINT AS THE 4GHZ BALUN, CAN BE USED.

07585-098

Figure 98. Evaluation Board Schematic

Table 5. Evaluation Board Configuration Options

Component	Description	Default Condition
VPOSx, GNDx	Power Supply and Ground Vector Pins.	Not applicable
R10x, R12x, R19x	Power Supply Decoupling. Shorts or power supply decoupling resistors.	R10x, R12x, R19x = 0 Ω (0603)
C6x to C11x	The capacitors provide the required dc coupling up to 6 GHz.	C6x, C7x, C8x = 100 pF (0402), C9x, C10x, C11x = 0.1 µF (0603)
P1x, R11x, R9x, R1x	Device Enable. When connected to V_S, the device is active.	P1x, R9x = DNI, R1x = DNI, R11x = 0 Ω
R23x	Adjust Pin. The resistor value here sets the bias voltage at this pin and optimizes third-order distortion.	R23B = 1.5 kΩ (0603), R23A = 200 Ω (0603)
C1x to C5x, C12x	AC Coupling Capacitors. These capacitors provide the required ac coupling from 400 MHz to 4 GHz.	C1x, C4x = DNI, C2x, C3x, C5x, C12x = 100 pF (0402)
R2x to R7x, R13x to R18x	Single-Ended Baseband Output Path. This is the default configuration of the evaluation board. R13x to R18x are populated for appropriate balun interface. R2x to R5x are not populated. Baseband outputs are taken from QHI and IHI. The user can reconfigure the board to use full differential baseband outputs. R2x to R5x provide a means to bypass the 9:1 TCM9-1 transformer to allow for differential baseband outputs. Access the differential baseband signals by populating R2x to R5x with 0 Ω and not populating R13x to R18x. This way the transformer does not need to be removed. The baseband outputs are taken from the SMAs of QHI, QLO, IHI, and ILO. R6x and R7x are provisions for applying a specific differential load across the baseband outputs	R2x to R7x = open, R13x to R18x = 0 Ω (0402)
T2x, T4x	IF Output Interface. TCM9-1 converts a differential high impedance IF output to a single-ended output. When loaded with 50 Ω, this balun presents a 450 Ω load to the device. The center tap can be decoupled through a capacitor to ground.	T2x, T4x = TCM9-1, 9:1 (Mini-Circuits)
C15x, C16x	Decoupling Capacitors. C15x and C16x are the decoupling capacitors used to reject noise on the center tap of the TCM9-1.	C15x, C16x = 0.1 µF (0402)
T1x	LO Input Interface. A 1:1 RF balun that converts the single-ended RF input to differential signal is used.	T1B = TC1-1-13, 1:1 (Mini-Circuits) for operation <3 GHz, T1A = Johanson Technology 3600BL14M050 for operation from 3 GHz to 4 GHz, Johanson Technology 5400BL15K050 for operation from 4900 MHz to 5800 MHz
T3x	RF Input Interface. A 1:1 RF balun that converts the single-ended RF input to differential signal is used.	T3B = TC1-1-13, 1:1 (Mini-Circuits) for operation <3 GHz, T3A = Johanson Technology 3600BL14M050 for operation from 3 GHz to 4 GHz, Johanson Technology 5400BL15K050 for operation from 4900 MHz to 5800 MHz

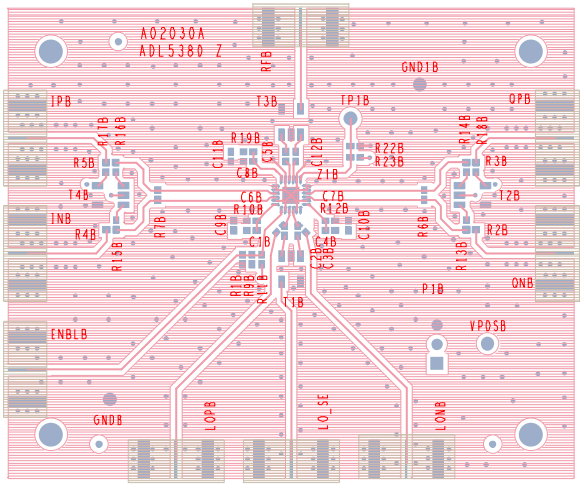


Figure 99. Low Band Evaluation Board Top Layer

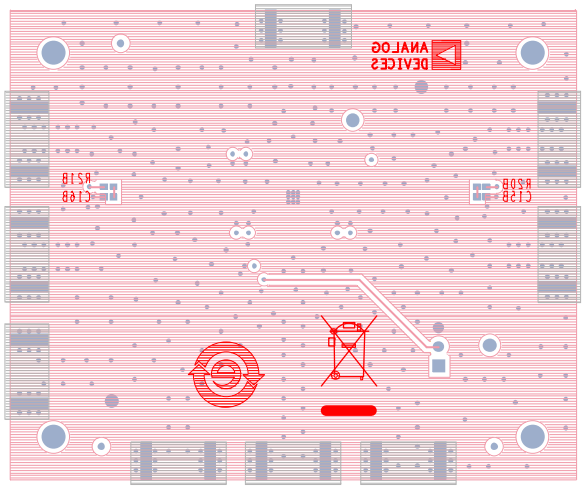


Figure 101. Low Band Evaluation Board Bottom Layer

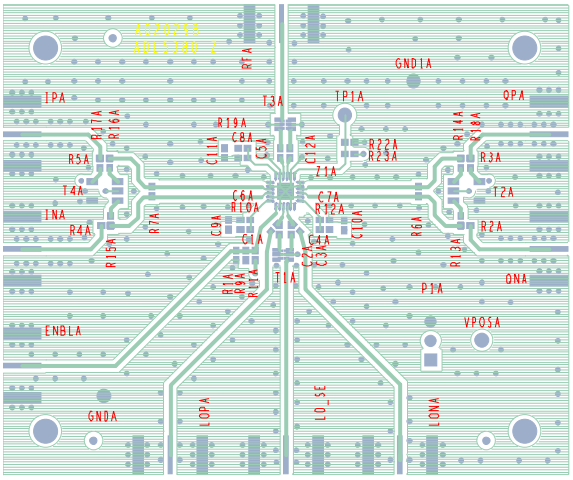


Figure 100. Midband/High Band Evaluation Board Top Layer Silkscreen

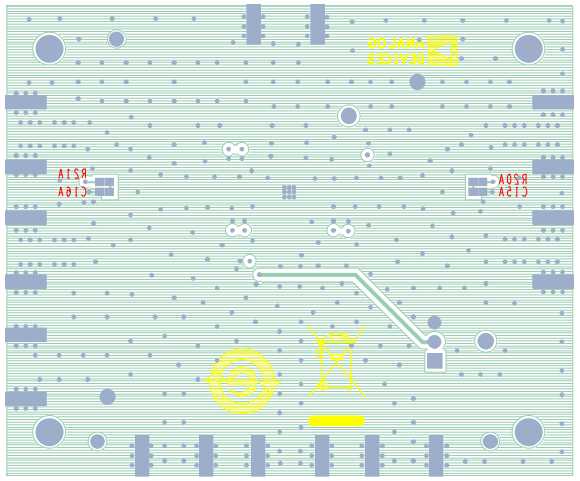


Figure 102. Midband/High Band Evaluation Board Bottom Layer Silkscreen

THERMAL GROUNDING AND EVALUATION BOARD LAYOUT

The package for the ADL5380 features an exposed paddle on the underside that should be well soldered to a low thermal and electrical impedance ground plane. This paddle is typically soldered to an exposed opening in the solder mask on the evaluation board. Figure 103 illustrates the dimensions used in the layout of the ADL5380 footprint on the ADL5380 evaluation board (1 mil = 0.0254 mm).

Notice the use of nine via holes on the exposed paddle. These ground vias should be connected to all other ground layers on the evaluation board to maximize heat dissipation from the device package.

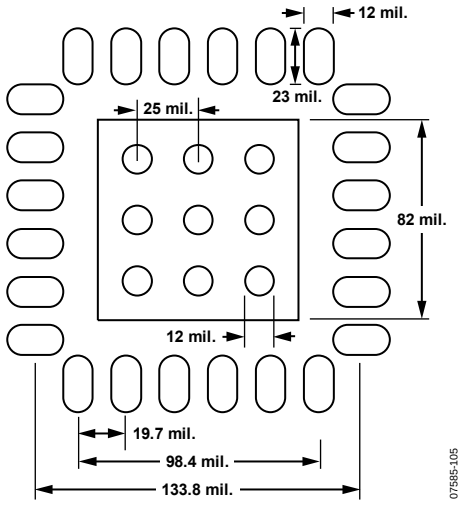


Figure 103. Dimensions for Evaluation Board Layout for the ADL5380 Package

Under these conditions, the thermal impedance of the ADL5380 was measured to be approximately 30°C/W in still air.

OUTLINE DIMENSIONS

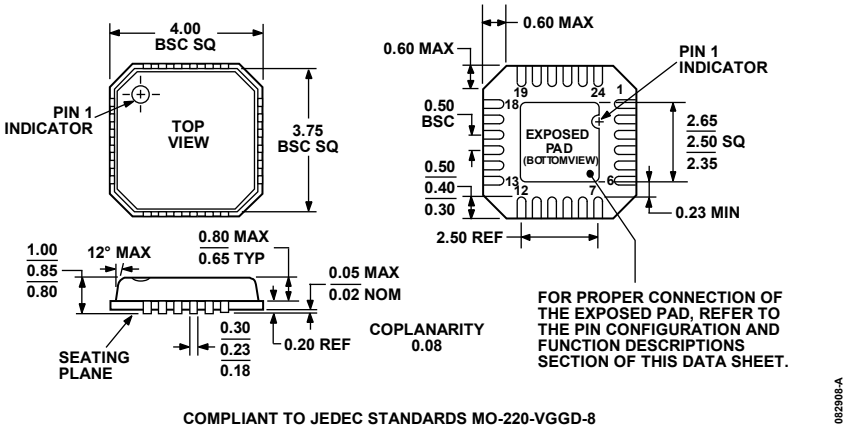


Figure 104. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5380ACPZ-R7[1]	–40°C to +85°C	24-Lead LFCSP_VQ	CP-24-3	1,500, 7″ Tape and Reel
ADL5380ACPZ-WP[1]	–40°C to +85°C	24-Lead LFCSP_VQ	CP-24-3	64, Waffle Pack
ADL5380-29A-EVALZ[1]		Mid Band (3 GHz to 4 GHz) Evaluation Board		1
ADL5380-30A-EVALZ[1]		Low Band (400 MHz to 3 GHz) Evaluation Board		1

[1] Z = RoHS Compliant Part.

NOTES

D07585-0-7/09(0)

High Current Output, Triple Video Amplifier

AD8023

FEATURES
Drives 13 V Output
Drives Unlimited Capacitive Load
High Current Output Drive: 70 mA
Excellent Video Specifications (R_L = 150 Ω)
Gain Flatness 0.1 dB to 10 MHz
0.06% Differential Gain Error
0.02° Differential Phase Error
Power
Operates on ±2.5 V to ±7.5 V Supply
10.0 mA/Amplifier Max Power Supply Current
High Speed
250 MHz Unity Gain Bandwidth (3 dB)
1200 V/μs Slew Rate
Fast Settling Time of 35 ns (0.1%)
High Speed Disable Function
Turn-Off Time 30 ns
Easy to Use
200 mA Short Circuit Current
Output Swing to 1 V of Rails

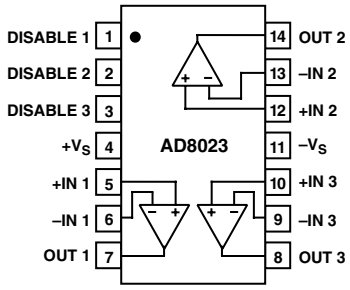
APPLICATIONS
LCD Displays
Video Line Driver
Broadcast and Professional Video
Computer Video Plug-In Boards
Consumer Video
RGB Amplifier in Component Systems

PRODUCT DESCRIPTION

The AD8023 is a high current output drive, high voltage output drive, triple video amplifier. Each amplifier has 70 mA of output current and is optimized for driving large capacitive loads. The amplifiers are current feedback amplifiers and feature gain flatness of 0.1 dB to 10 MHz while offering differential gain and phase error of 0.06% and 0.02°.

PIN CONFIGURATION

14-Lead SOIC



The AD8023 uses maximum supply current of 10.0 mA per amplifier and runs on ±2.5 V to ±7.5 V power supply. The outputs of each amplifier swing to within one volt of either supply rail to easily accommodate video signals. The AD8023 is unique among current feedback op amps by virtue of its large capacitive load drive with a small series resistor, while still achieving rapid settling time. For instance, it can settle to 0.1% in 35 ns while driving 300 pF capacitance.

The bandwidth of 250 MHz along with a 1200 V/μs slew rate make the AD8023 useful in high speed applications requiring a single +5 V or dual power supplies up to ±7.5 V. Furthermore, the AD8023 contains a high speed disable function for each amplifier in order to power down the amplifier or high impedance the output. This can then be used in video multiplexing applications. The AD8023 is available in the industrial temperature range of –40°C to +85°C.

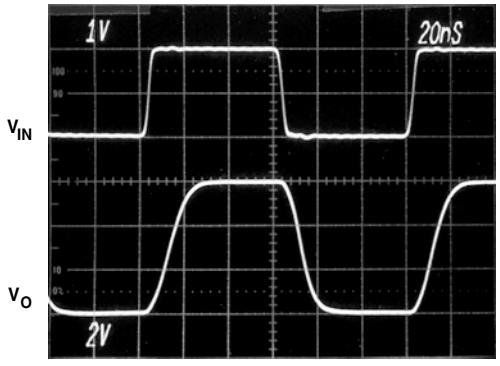


Figure 1. Pulse Response Driving a Large Load Capacitor, C_L = 300 pF, G = +3, R_F = 750 Ω, R_S = 16.9 Ω, R_L = 10 kΩ

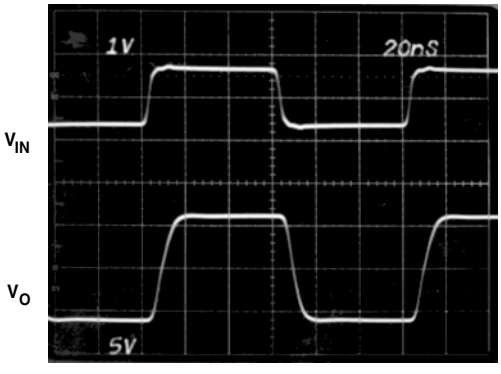


Figure 2. Output Swing Voltage, R_L = 150 Ω; V_S = ±7.5 V, G = +10

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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Fax: 781/326-8703

AD8023—SPECIFICATIONS (@ T_A = +25°C, V_S = ±7.5, C_{LOAD} = 10 pF, R_{LOAD} = 150 Ω, unless otherwise noted)

Model	Conditions	V_S	AD8023A Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
Bandwidth (3 dB)	R_{FB} = 750 Ω No Peaking, G = +3			125		MHz
Bandwidth (0.1 dB)	No Peaking, G = +3			7		MHz
Slew Rate	5 V Step			1200		V/µs
Settling Time to 0.1%	0 V to ±6 V (6 V Step)					
	C_{LOAD} = 300 pF					
	R_{LOAD} > 1 kΩ, R_{FB} = 750 Ω					
	T_A = +25°C to +70°C, R_S = 16.9 Ω			30		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion						
	f_C = 5 MHz, R_L = 150 Ω, V_O = 2 p-p			–72		dBc
Input Voltage Noise	f = 10 kHz			2.0		nV/√Hz
Input Current Noise	f = 10 kHz ($-I_{IN}$)			14		pA/√Hz
Differential Gain (R_L = 150 Ω)	f = 3.58 MHz, G = +2, R_{FB} = 750 Ω			0.06		%
Differential Phase (R_L = 150 Ω)	f = 3.58 MHz, G = +2, R_{FB} = 750 Ω			0.02		Degrees
DC PERFORMANCE						
Input Offset Voltage	T_{MIN} to T_{MAX}		–5	2	5	mV
Offset Drift				2		µV/°C
Input Bias Current (–)	T_{MIN} to T_{MAX}		–45	15	45	µA
Input Bias Current (+)	T_{MIN} to T_{MAX}		–25	5	25	µA
Open-Loop Transresistance			67	111		kΩ
	T_{MIN} to T_{MAX}		50	111		kΩ
INPUT CHARACTERISTICS						
Input Resistance						
+Input	T_{MIN} to T_{MAX}			100		kΩ
–Input	T_{MIN} to T_{MAX}			75		Ω
Input Capacitance				2		pF
Input Common-Mode Voltage Range				±6.0		V
Common-Mode Rejection Ratio						
Input Offset Voltage			50	56		dB
–Input Current				0.2		µA/V
+Input Current				5		µA/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing						
R_L = 1 kΩ	V_{OL}–V_{EE}			0.8	1.0	V
	V_{CC}–V_{OH}			0.8	1.0	V
R_L = 150 Ω	V_{OL}–V_{EE}			1.0	1.3	V
	V_{CC}–V_{OH}			1.0	1.3	V
Output Current			50	70		mA
Short-Circuit Current				300		mA
Capacitive Load Drive				1000		pF
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	G = +2, f = 5 MHz			70		dB
DC						
Input Offset Voltage			–5	0.3	5	mV
–Input Bias Current			–10	3	10	µA
POWER SUPPLY						
Operating Range	Single Supply		+4.2		+15	V
	Dual Supply		±2.1		±7.5	V
Quiescent Current/Amplifier				6.2		mA
				7.0	10.0	mA
	T_{MIN} to T_{MAX}					
	Power-Down			1.3	4.0	mA

Model	Conditions	V_S	AD8023A Min	Typ	Max	Units
POWER SUPPLY (Continued)						
Power Supply Rejection Ratio	V_S = ±2.5 V to ±7.5 V					dB
Input Offset Voltage			54	76		dB
–Input Current				0.03		µA/V
+Input Current				0.07		µA/V
DISABLE CHARACTERISTICS						
Off Isolation	f = 6 MHz			–70		dB
Off Output Capacitance	G = +1			12		pF
Turn-On Time				50		ns
Turn-Off Time	R_L = 150 Ω			30		ns
Switching Threshold		$V_{TH} - V_{EE}$		1.6		V

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . 15.5 V Total
Internal Power Dissipation
Small Outline (R) . . . . 1.0 Watts (Observe Derating Curves)
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±3 V (Clamped)
Output Voltage Limit
Maximum . . . . . $+V_S$
Minimum . . . . . $-V_S$
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range
R Package . . . . . –65°C to +125°C
Operating Temperature Range
AD8023A . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8023AR	–40°C to +85°C	14-Lead Plastic SOIC	R-14
AD8023AR-REEL	–40°C to +85°C	13" Tape and Reel	R-14
AD8023AR-REEL7	–40°C to +85°C	7" Tape and Reel	R-14
AD8023ACHIPS	–40°C to +85°C	Die	

Maximum Power Dissipation

The maximum power that can be safely dissipated by the AD8023 is limited by the associated rise in junction temperature. The maximum safe junction temperature for the plastic encapsulated parts is determined by the glass transition temperature of the plastic, about 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8023 is internally short circuit protected, this may not be enough to guarantee that the maximum junction temperature is not exceeded under all conditions. To ensure proper operation, it is important to observe the derating curves.

It must also be noted that in (noninverting) gain configurations (with low values of gain resistor), a high level of input overdrive can result in a large input error current, which may result in a significant power dissipation in the input stage. This power must be included when computing the junction temperature rise due to total internal power.

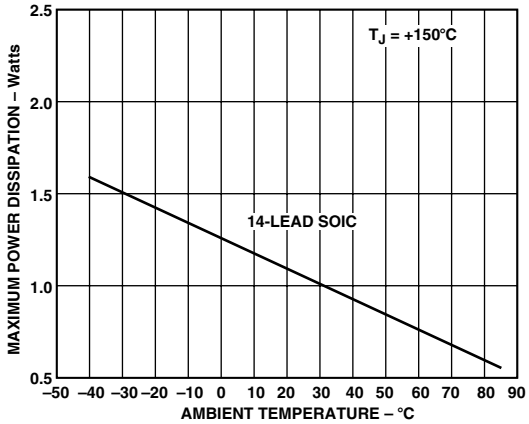


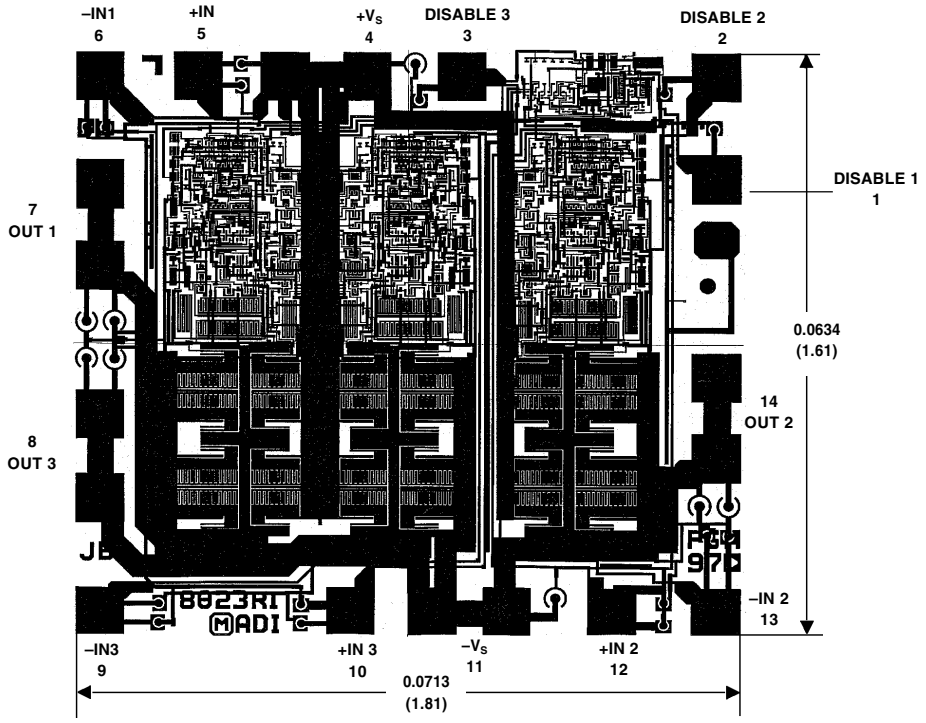
Figure 3. Maximum Power Dissipation vs. Ambient Temperature

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8023 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

METALIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Typical Performance Characteristics

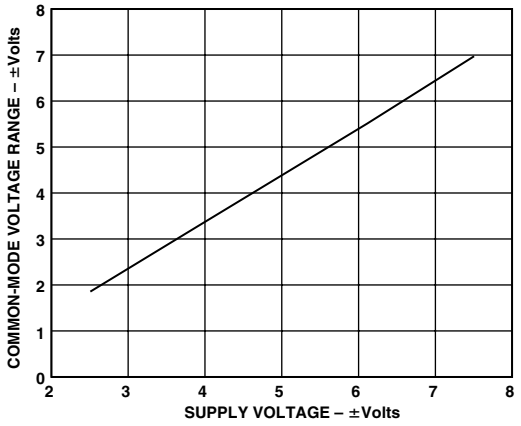


Figure 4. Input Common-Mode Voltage Range vs. Supply Voltage

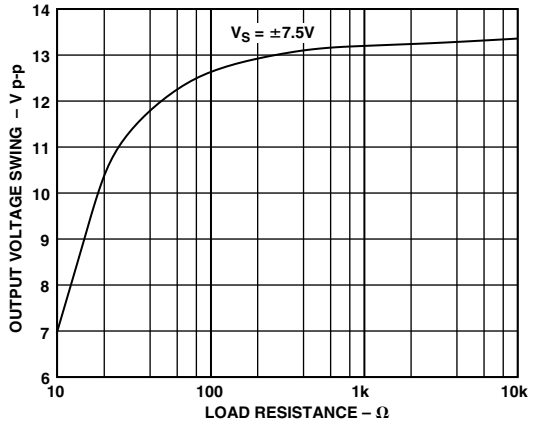


Figure 5. Output Voltage Swing vs. Load Resistance

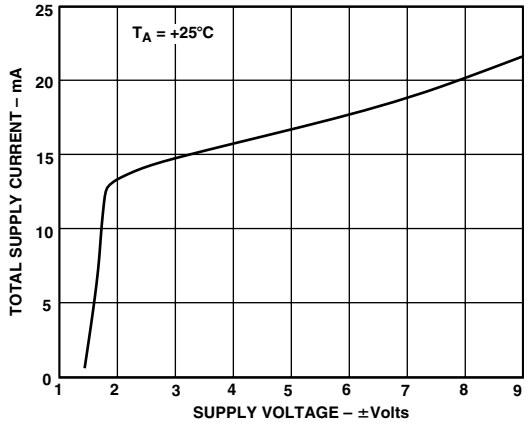


Figure 6. Total Supply Current vs. Supply Voltage

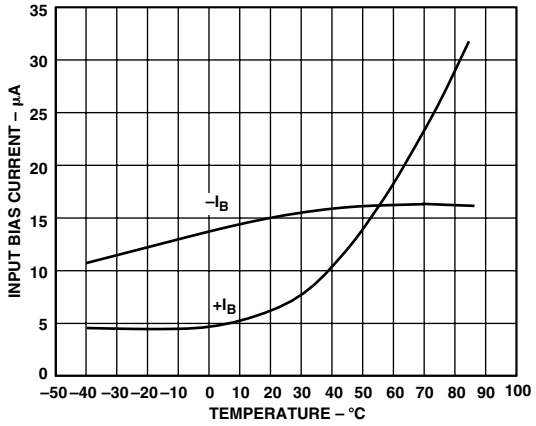


Figure 9. Input Bias Current vs. Temperature

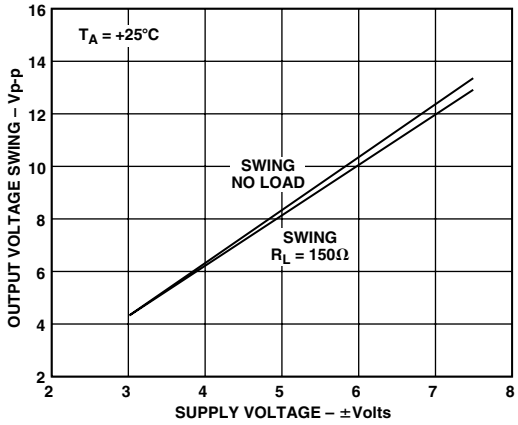


Figure 7. Output Voltage Swing vs. Supply Voltage

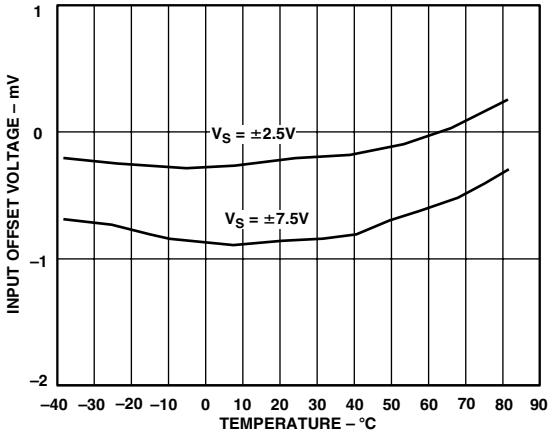


Figure 10. Input Offset Voltage vs. Temperature

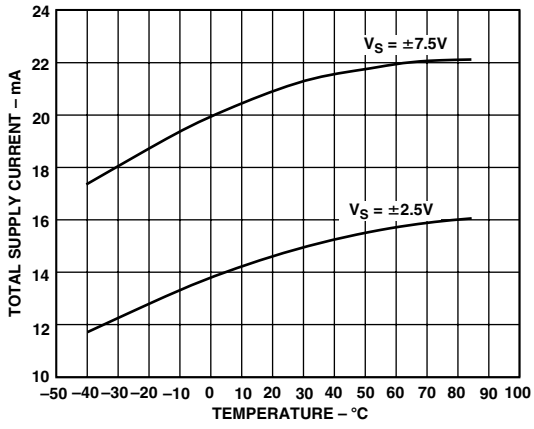


Figure 8. Total Supply Current vs. Temperature

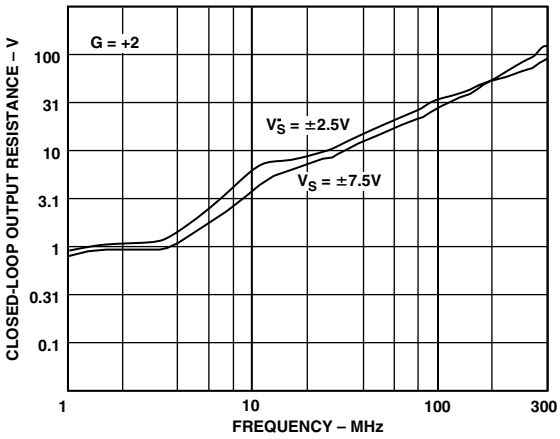


Figure 11. Closed-Loop Output Resistance vs. Frequency

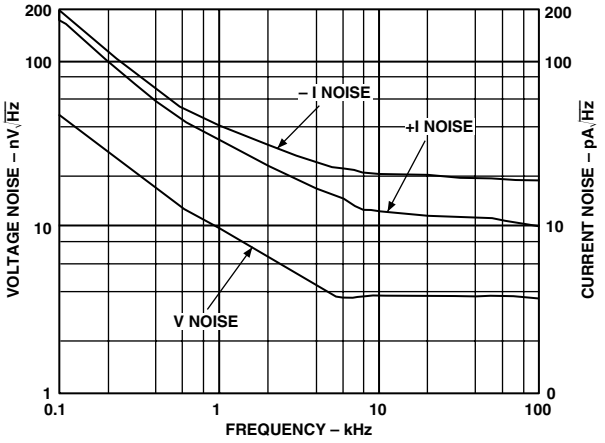


Figure 12. Input Current and Voltage Noise vs. Frequency

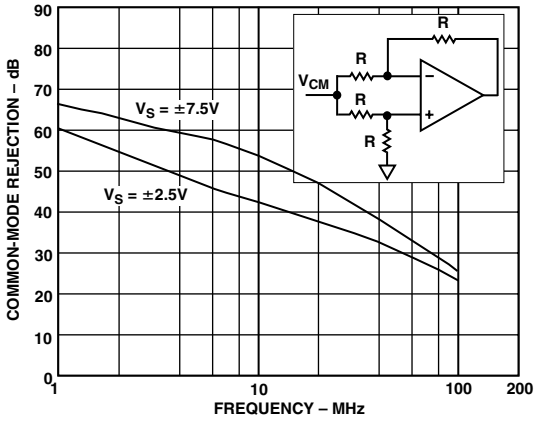


Figure 15. Common-Mode Rejection vs. Frequency

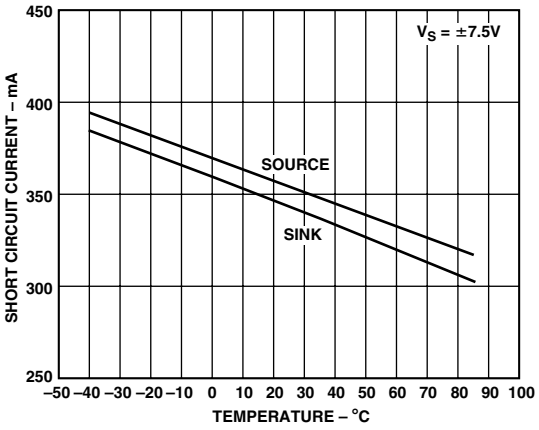


Figure 13. Short Circuit Current vs. Temperature

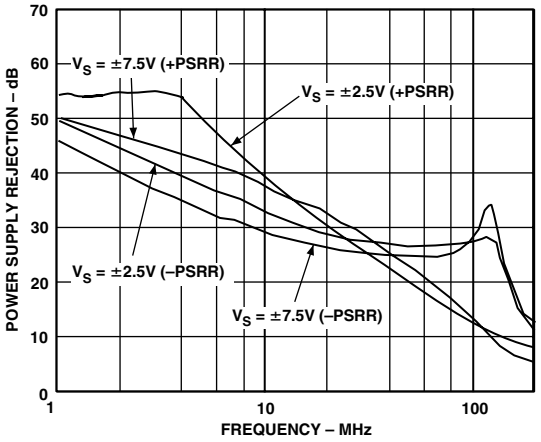


Figure 16. Power Supply Rejection Ratio vs. Frequency

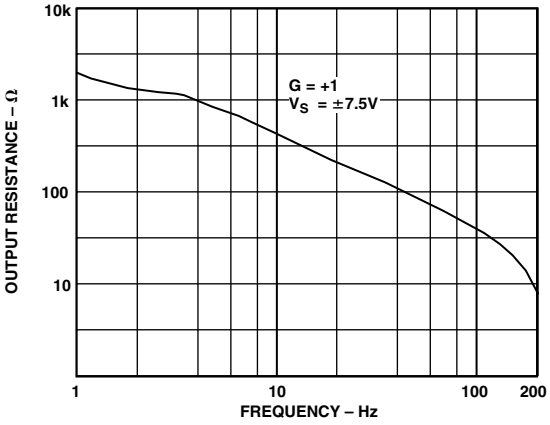


Figure 14. Output Resistance vs. Frequency, Disabled State

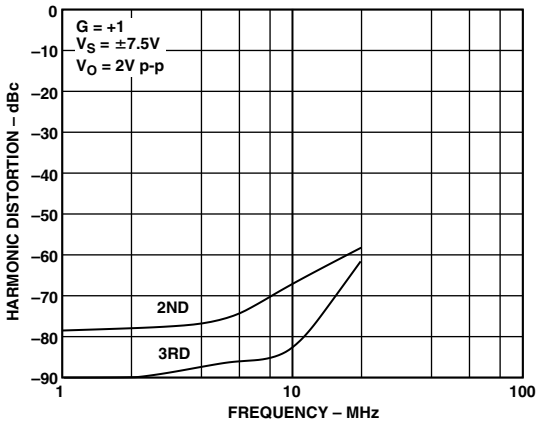


Figure 17. Harmonic Distortion vs. Frequency, R_L = 150 Ω

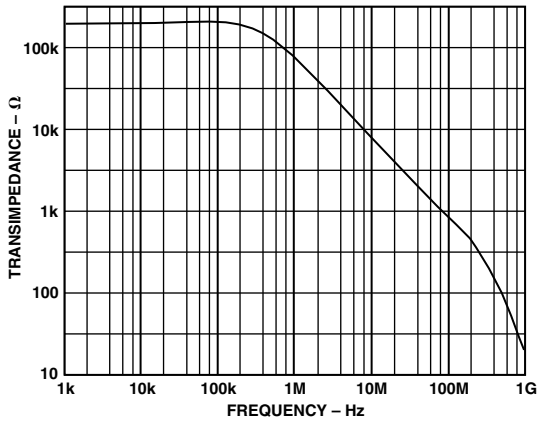


Figure 18. Open-Loop Transimpedance vs. Frequency

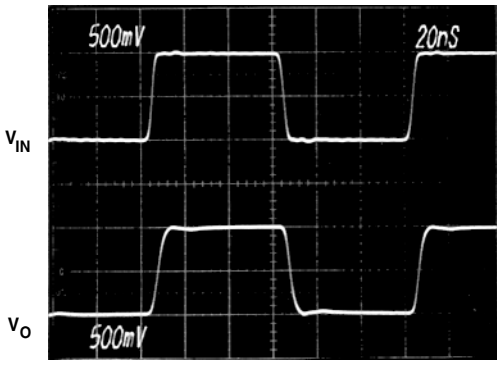


Figure 21. Small Signal Pulse Response, Gain = +1, (R_F = 2 kΩ, R_L = 150 Ω, V_S = ±7.5 V)

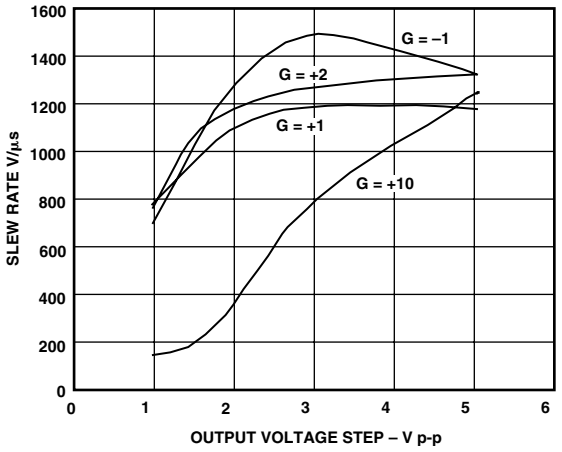


Figure 19. Slew Rate vs. Output Step Size

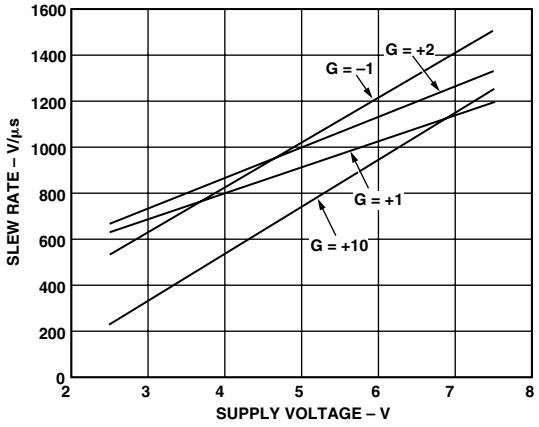


Figure 22. Maximum Slew Rate vs. Supply Voltage

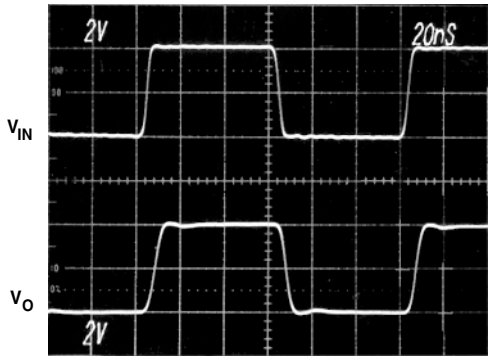


Figure 20. Large Signal Pulse Response, Gain = +1, (R_F = 2 kΩ, R_L = 150 Ω, V_S = ±7.5 V)

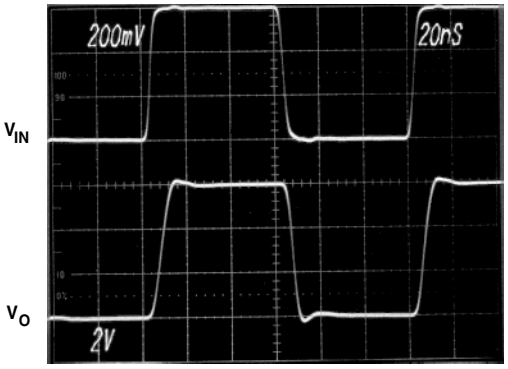


Figure 23. Large Signal Pulse Response, Gain = +10, (R_F = 274 Ω, R_L = 150 Ω, V_S = ±7.5 V)

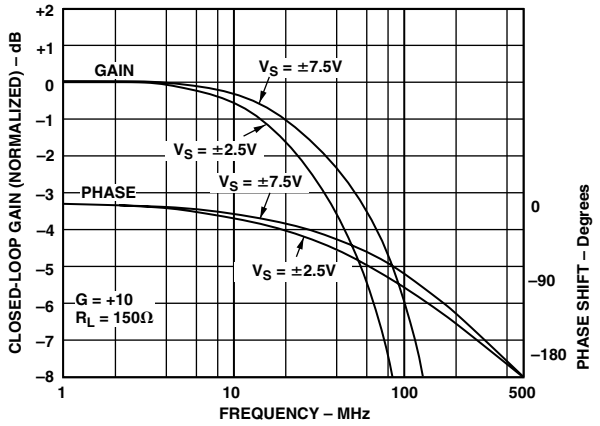


Figure 24. Closed-Loop Gain and Phase vs. Frequency, G = +10, R_L = 150 Ω

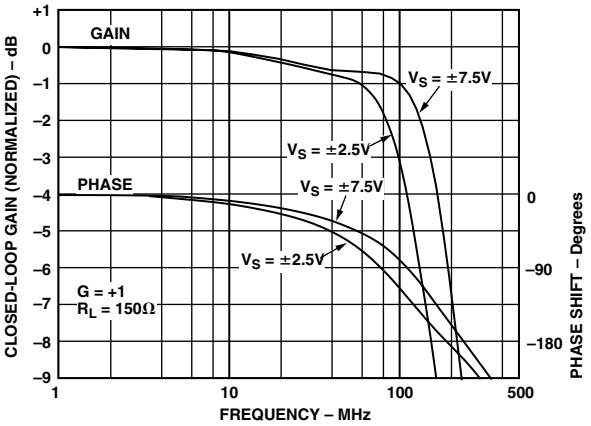


Figure 27. Closed-Loop Gain and Phase vs. Frequency, G = –1, R_L = 150 Ω

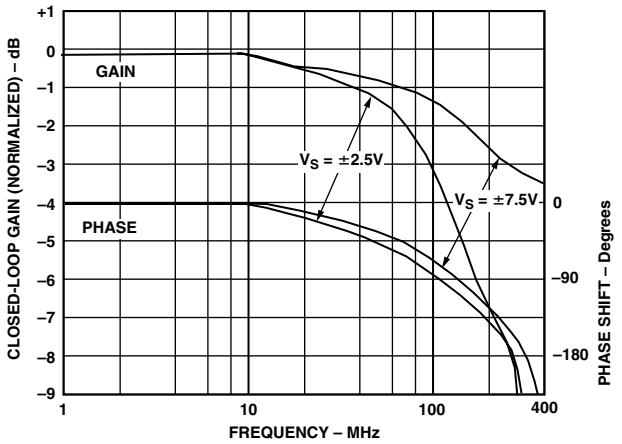


Figure 25. Closed-Loop Gain and Phase vs. Frequency, G = +1, R_L = 150 Ω

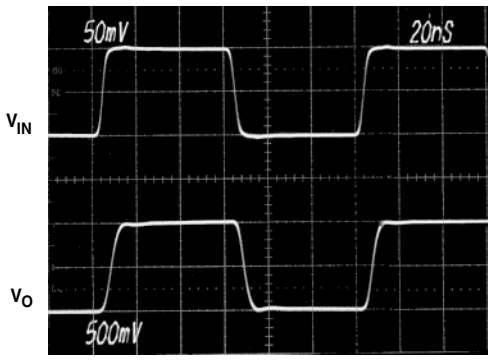


Figure 28. Small Signal Pulse Response, Gain = +10, (R_F = 274 Ω, R_L = 150 Ω, V_S = ±7.5 V)

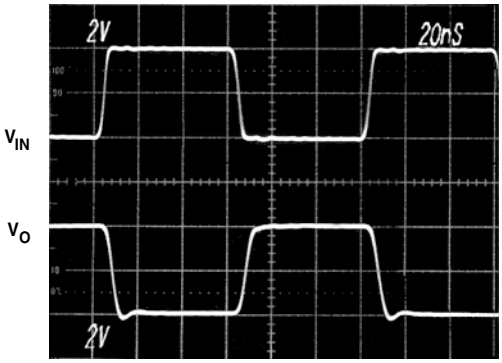


Figure 26. Large Signal Pulse Response, Gain = –1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±7.5 V)

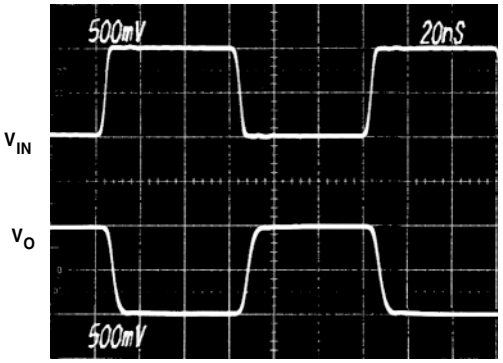


Figure 29. Small Signal Pulse Response, Gain = –1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±7.5 V)

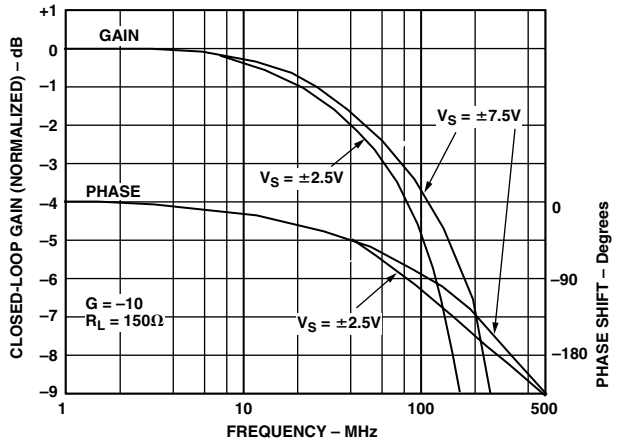


Figure 30. Closed-Loop Gain and Phase vs. Frequency, G = –10, R_L = 150 Ω

General

The AD8023 is a wide bandwidth, triple video amplifier that offers a high level of performance on less than 9.0 mA per amplifier of quiescent supply current. The AD8023 achieves bandwidth in excess of 200 MHz, with low differential gain and phase errors and high output current making it an efficient video amplifier.

The AD8023's wide phase margin coupled with a high output short circuit current make it an excellent choice when driving any capacitive load up to 300 pF.

It is designed to offer outstanding functionality and performance at closed-loop inverting or noninverting gains of one or greater.

Choice of Feedback and Gain Resistors

Because it is a current feedback amplifier, the closed-loop bandwidth of the AD8023 may be customized using different values of the feedback resistor. Table I shows typical bandwidths at different supply voltages for some useful closed-loop gains when driving a load of 150 Ω.

The choice of feedback resistor is not critical unless it is desired to maintain the widest, flattest frequency response. The resistors recommended in the table (chip resistors) are those that will result in the widest 0.1 dB bandwidth without peaking. In applications requiring the best control of bandwidth, 1% resistors are adequate. Resistor values and widest bandwidth figures are shown. Wider bandwidths than those in the table can be attained by reducing the magnitude of the feedback resistor (at the expense of increased peaking), while peaking can be reduced by increasing the magnitude of the feedback resistor.

Increasing the feedback resistor is especially useful when driving large capacitive loads as it will increase the phase margin of the closed-loop circuit. (Refer to the Driving Capacitive Loads section for more information.)

To estimate the –3 dB bandwidth for closed-loop gains of 2 or greater, for feedback resistors not listed in the following table, the following single pole model for the AD8023 may be used:

$$ACL \simeq \frac{G}{1 + SC_T\,(R_F + Gn\,rin)}$$

where: C_T = transcapacitance ≅ 1 pF
R_F = feedback resistor
G = ideal closed loop gain

$$Gn = \left(1 + \frac{R_F}{R_G}\right) = \text{noise gain}$$

rin = inverting input resistance ≅ 150 Ω
ACL = closed loop gain

The –3 dB bandwidth is determined from this model as:

$$f_3 \simeq \frac{1}{2\,\pi\,C_T(R_F + Gn\,rin)}$$

This model will predict –3 dB bandwidth to within about 10% to 15% of the correct value when the load is 150 Ω and V_S = ±7.5 V. For lower supply voltages there will be a slight decrease in bandwidth. The model is not accurate enough to predict either the phase behavior or the frequency response peaking of the AD8023.

It should be noted that the bandwidth is affected by attenuation due to the finite input resistance. Also, the open-loop output resistance of about 6 Ω reduces the bandwidth somewhat when driving load resistors less than about 150 Ω. (Bandwidths will be about 10% greater for load resistances above a couple hundred ohms.)

Table I. –3 dB Bandwidth vs. Closed-Loop Gain and Feedback Resistor, R_L = 150 Ω (SOIC)

V_S – Volts	Gain	R_F – Ohms	BW – MHz
±7.5	+1	2000	460
	+2	750	240
	+10	300	50
	–1	750	150
	–10	250	60
±2.5	+1	2000	250
	+2	1000	90
	+10	300	30
	–1	750	95
	–10	250	50

Driving Capacitive Loads

When used in combination with the appropriate feedback resistor, the AD8023 will drive any load capacitance without oscillation. The general rule for current feedback amplifiers is that the higher the load capacitance, the higher the feedback resistor required for stable operation. Due to the high open-loop transresistance and low inverting input current of the AD8023, the use of a large feedback resistor does not result in large closed-loop gain errors. Additionally, its high output short circuit current makes possible rapid voltage slewing on large load capacitors.

For the best combination of wide bandwidth and clean pulse response, a small output series resistor is also recommended. Table II contains values of feedback and series resistors which result in the best pulse responses. Figure 28 shows the AD8023 driving a 300 pF capacitor through a large voltage step with virtually no overshoot. (In this case, the large and small signal pulse responses are quite similar in appearance.)

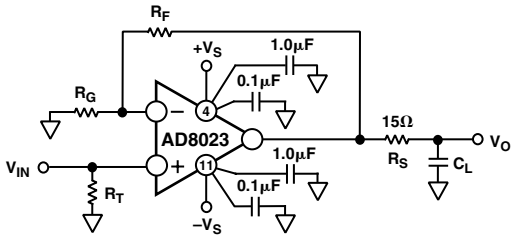


Figure 31. Circuit for Driving a Capacitive Load

Table II. Recommended Feedback and Series Resistors vs. Capacitive Load and Gain

C_L – pF	R_F – Ohms	R_S – Ohms G = 2	R_S – Ohms G ≥ 3
20	2k	0	0
50	2k	10	10
100	2k	15	15
200	3k	10	10
300	3k	10	10
≥500	3k	10	10

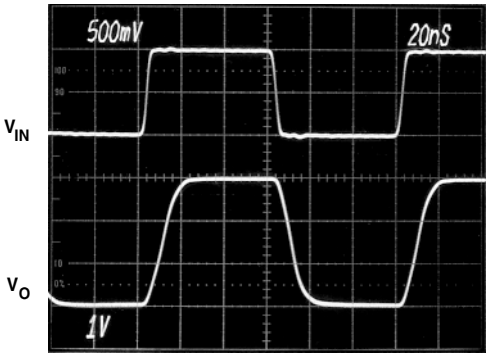


Figure 32. Pulse Response Driving a Large Load Capacitor. C_L = 300 pF, G = +3, R_F = 750 Ω, R_S = 16.9 Ω, R_L = 10 kΩ

Overload Recovery

The three important overload conditions are: input common-mode voltage overdrive, output voltage overdrive, and input current overdrive. When configured for a low closed-loop gain, this amplifier will quickly recover from an input common-mode voltage overdrive; typically in under 25 ns. When configured for a higher gain, and overloaded at the output, the recovery time will also be short. For example, in a gain of +10, with 50% overdrive, the recovery time of the AD8023 is about 20 ns (see Figure 31). For higher overdrive, the response is somewhat slower. For 100% overdrive, (in a gain of +10), the recovery time is about 80 ns.

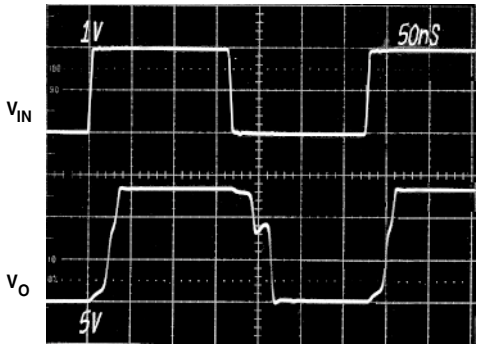


Figure 33. 50% Overload Recovery, Gain = +10, (R_F = 300 Ω, R_L = 1 kΩ, V_S = ±7.5 V)

As noted in the warning under Maximum Power Dissipation, a high level of input overdrive in a high noninverting gain circuit can result in a large current flow in the input stage. Though this current is internally limited to about 30 mA, its effect on the total power dissipation may be significant.

Disable Mode Operation

Pulling the voltage on any one of the Disable pins about 1.6 V up from the negative supply will put the corresponding amplifier into a disabled, powered down, state. In this condition, the amplifier's quiescent current drops to about 1.3 mA, its output becomes a high impedance, and there is a high level of isolation from input to output. In the case of a gain of two line driver for example, the impedance at the output node will be about the same as for a 1.5 kΩ resistor (the feedback plus gain resistors) in parallel with a 12 pF capacitor.

Leaving the Disable pin disconnected (floating) will leave the corresponding amplifier operational, in the enabled state. The input impedance of the disable pin is about 25 kΩ in parallel with a few picofarads. When driven to 0 V, with the negative supply at –7.5 V, about 100 µA flows into the disable pin.

When the disable pins are driven by complementary output CMOS logic, on a single 5 V supply, the disable and enable times are about 50 ns. When operated on dual supplies, level shifting will be required from standard logic outputs to the Disable pins. Figure 33 shows one possible method, which results in a negligible increase in switching time.

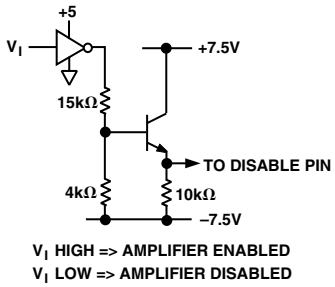


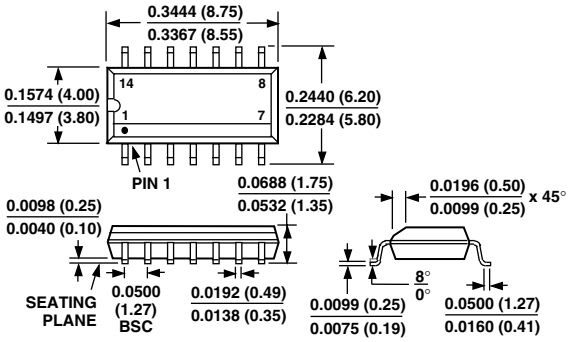
Figure 34. Level Shifting to Drive Disable Pins on Dual Supplies

The AD8023's input stages include protection from the large differential input voltages that may be applied when disabled. Internal clamps limit this voltage to about ±3 V. The high input to output isolation will be maintained for voltages below this limit.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Plastic SOIC
(R-14)



C3137–0–3/00 (rev. A)

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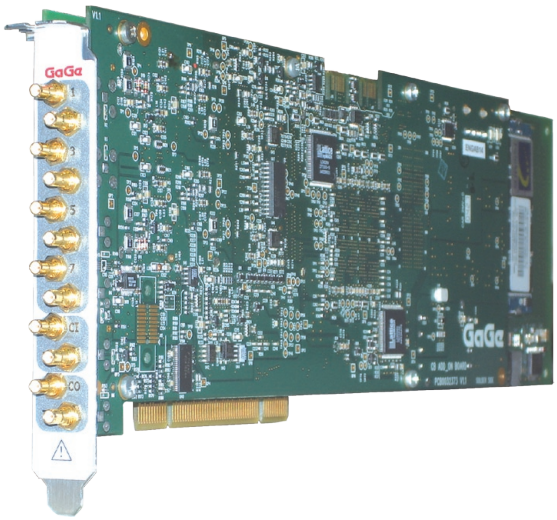
Octopus CompuScope 83XX

14-Bit Family of Multi-channel Digitizers for the PCI Bus

The GaGe Octopus™ family of multi-channel digitizers features up to 8 channels in a single-slot PCI card with up to 125 MS/s sampling per channel, and up to 4 GB of on-board acquisition memory. Combine several Octopus cards for up to 64 channels in a single system.

With more than 35 new digitizers to choose from, we offer you many more options than ever before.



The Octopus family represents a new generation of GaGe digitizers that has all of the advanced features you would expect from a top performance signal capture card:

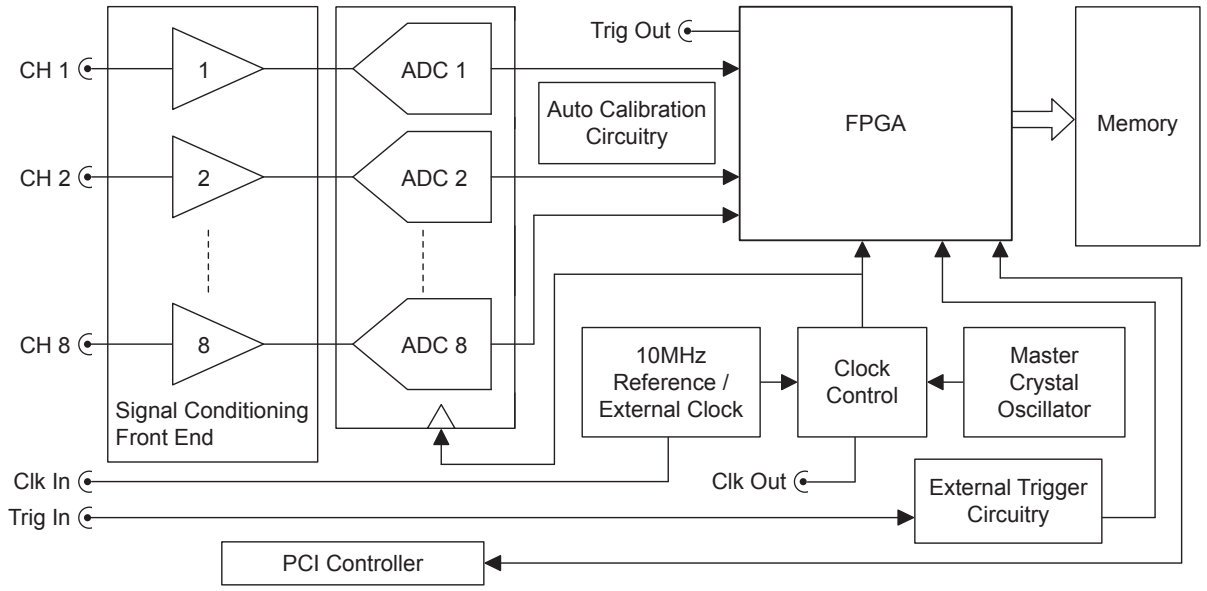
FEATURES

- 2, 4, or 8 digitizing channels
- 10, 25, 50, 65, 100, or 125 MS/s sampling per channel
- 14 bits vertical resolution
- 128 MS to 2 GS on-board acquisition memory
- More than 100 MHz bandwidth
- Full-size, single-slot PCI card
- Full-featured front-end, with software control over input ranges, coupling and impedances
- 32 bits, 66 MHz PCI standard for 200 MB/s transfer to PC memory
- Ease of integration with External or Reference Clock In and Clock Out, External Trigger In and Trigger Event Out
- Programming-free operation with GageScope® oscilloscope software
- Software Development Kits available for LabVIEW, MATLAB, C/C#

APPLICATIONS

Radar Design and Test
Disk Drive Testing
Manufacturing Test
Signal Intelligence
Lidar Systems
Communications
Non-Destructive Testing
Spectroscopy
High-Performance Imaging
Ultrasound Test

Octopus CompuScope 83XX Simplified Block Diagram



A/D SAMPLING

Number of Inputs:	2, 4 or 8
Resolution:	14 bits
ENOB (see Note 1):	10.7 bits
SNR (see Note 1):	66 dB
SFDR (see Note 1):	72 dB
SINAD (see Note 1):	65 dB
Maximum Sampling Rate Per Channel (product-dependent):	10, 25, 50, 65, 100 or 125 MS/s
Sampling Rates:	125 MS/s, 105 MS/s, 100 MS/s, 80 MS/s, 65 MS/s, 50 MS/s, 40 MS/s, 25 MS/s, 20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 kS/s, 200 kS/s, 100 kS/s, 50 kS/s 20 kS/s, 10 kS/s, 5 kS/s, 2 kS/s, 1 kS/s
Connector:	SMB
Impedance:	1 MΩ or 50 Ω; (software-selectable)
Coupling:	AC or DC; (software-selectable)
AC Coupled Bandwidth:	10 Hz to >100 MHz (see Note 2)
DC Coupled Bandwidth:	DC to >200 MHz (50 Ω only, see Note 5)
Flatness (see Note 3):	Within ±0.5 dB of ideal response to 40 MHz
DC Accuracy (see Note 4):	±0.5 %
Input Voltage Ranges:	±100 mV, ±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V (±5 V is only available in 50 Ω)
Protection:	
with 1 MΩ impedance:	Diode-clamped
with 50 Ω impedance:	Protection with 50 Ω source impedance
Absolute Maximum Amplitude	
with 1 MΩ impedance:	±15 V (continuous)
with 50 Ω impedance:	±5 V (continuous)

LOW-PASS FILTER

Type:	3-pole Bessel, 1 per channel
Cut-off Frequency:	20 MHz
Operation:	Individually software-selectable

ACQUISITION MEMORY

Active Channels	Total On-board Memory				
	128 M	256 M	512 M	1 G	2 G
1	128 M	256 M	512 M	1 G	2 G
2	64 M	128 M	256 M	512 M	1 G
4	32 M	64 M	128 M	256 M	512 M
8	16 M	32 M	64 M	128 M	256 M

TRIGGERING

Trigger Engines:	2 per channel, 1 for external trigger
Source:	CH 1 to 8, EXT or Software
Input Combination:	All combinations of sources logically OR'ed
Trigger Level Accuracy:	Less than ±2% of Full Scale for channel triggering
Slope:	Positive or Negative; software-selectable
Sensitivity:	±2% of Full Scale This implies that signal amplitude must be at least 4% of full scale to cause a trigger to occur. Smaller signals are rejected as noise.
Post-Trigger Data:	128 points minimum. Can be defined with a 64 point resolution.
Maximum Record Length:	Maximum memory depth

EXTERNAL TRIGGER

Impedance:	2 kΩ
Amplitude:	Absolute maximum ±15 V
Voltage Range:	±1 V, ±5 V (software-selectable)
Bandwidth:	>100 MHz
Coupling:	AC or DC
Connector:	SMB

TRIGGER OUT

Impedance:	50 Ω compatible
Amplitude:	0-2.5 V
Connector:	SMB

INTERNAL CLOCK

Accuracy:	±1 ppm (0 to 50°C ambient)

EXTERNAL CLOCK

Maximum Frequency:	Maximum product sample rate
Minimum Frequency:	2 MHz
Signal Level:	Minimum 1 V RMS Maximum 2 V RMS
Termination Impedance:	50 Ω
Sampling Edge:	Rising
Duty Cycle:	50% ±5%
Connector:	SMB
Coupling:	AC

EXTERNAL REFERENCE

The External Reference timebase is used to synchronize the Internal Sampling Clock

Frequency:	10 MHz ±1000 ppm; (software-selectable)
Signal Level:	Minimum 1 V RMS Maximum 2 V RMS
Impedance:	50 Ω
Sampling Edge:	Rising
Duty Cycle:	50% ±5%
Connector:	SMB

CLOCK OUT

Maximum Frequency:	Maximum product sample rate
Minimum Frequency:	2 MHz (from External Clock) 1 kHz (from Internal Clock)
Signal Level:	0-2.5 V
Impedance:	50 Ω compatible
Duty Cycle:	50% ±10%
Connector:	SMB

MULTIPLE RECORD

Pre-trigger Data:	Up to virtually full record length
Record Length:	128 points minimum. Can be defined with a 64 points resolution.

TIMESTAMPING

Resolution:	One sampling interval
Counter turnover:	>24 hours continuous

CARD SIZE

Single-slot, full-length PCI

SYSTEM REQUIREMENTS

PCI-based computer, minimum Pentium II 500 MHz, with at least one free full-length PCI slot, 128 MB RAM, 100 MB hard disk.

COOLING SYSTEM

Minimum CFM Requirement: *Characterization in progress*

†POWER (IN WATTS, PER CARD)

25.0 W (typical)

†Measured on a typical 4-channel Octopus card.

PCI BUS INTERFACE

Plug-&-Play:	Fully supported
Bus Mastering:	Fully supported
Scatter-Gather:	Fully supported
Bus Width:	32 bits
Bus Speed:	66 MHz or 33 MHz
Bus Throughput:	200 MB/s to PC memory (66 MHz PCI; dependent on motherboard and number of PCI-PCI bridges)
Compatibility:	PCI-compliant, v.2.2 Also v.2.1 systems that supply 3.3 V to PCI slot

MULTI-CARD SYSTEMS

Supported by all Octopus CompuScope models, GageScope, and SDKs.

OPERATING SYSTEMS

Windows XP:	All Versions
Windows 2000:	SP1 or higher

APPLICATION SOFTWARE

GageScope: Windows-based software for programming-free operation

LITE Edition:	Included with purchase, provides basic functionality
Standard Edition:	Provides limited functionality of advanced analysis tools, except for Extended Math
Professional Edition:	Provides full functionality of all advanced analysis tools

SOFTWARE DEVELOPMENT KITS (SDK)

CompuScope SDK for C/C# for Windows*

CompuScope SDK for MATLAB for Windows

CompuScope SDK for LabVIEW for Windows

*C/C# SDK is compatible with LabWindows/CVI 7.0+ compiler. Visual Basic.NET support available with purchase of C/C# SDK.

Contact your GaGe Sales Agent for information on Linux support.

WARRANTY

One year parts and labor

Certificate of NIST Traceable Calibration is included.

All specifications subject to change without notice.

Notes to specifications:

1) Measured at 125 MS/s in the ±500 mV range with 50 Ω input impedance using a 10 MHz sine wave with an amplitude of 95% of full scale and the on-board filtering capability.
2) 10 Hz at 1 MΩ only.
3) Measured at 125 MS/s in the ±500 mV range with 50 Ω input impedance with an amplitude of 95% of full scale.
4) Measured on ±500 mV, ±1 V, ±2 V input ranges for both 50 Ω and 1 MΩ input impedance settings.
5) Measured on ±1 V, ±2 V, ±5 V input ranges using the 50 Ω input impedance setting.

Unless otherwise specified, all dynamic performance specs have been qualified on engineering boards.

ORDERING INFORMATION

Hardware & Upgrades

Octopus 14-bit Family	2 Channel	4 Channel	8 Channel
10 MS/s	CS8320: OCT-832-000	CS8340: OCT-834-000	CS8380: OCT-838-000
25 MS/s	CS8322: OCT-832-002	CS8342: OCT-834-002	CS8382: OCT-838-002
50 MS/s	CS8324: OCT-832-004	CS8344: OCT-834-004	CS8384: OCT-838-004
65 MS/s	CS8325: OCT-832-005	CS8345: OCT-834-005	CS8385: OCT-838-005
100 MS/s	CS8327: OCT-832-007	CS8347: OCT-834-007	CS8387: OCT-838-007
125 MS/s	CS8329: OCT-832-009	CS8349: OCT-834-009	CS8389: OCT-838-009

Memory Upgrade: 128 MS to 256 MS	OCT-181-001
Memory Upgrade: 128 MS to 512 MS	OCT-181-003
Memory Upgrade: 128 MS to 1 GS	OCT-181-005
Memory Upgrade: 128 MS to 2 GS	OCT-181-007
36" SMB to BNC male cable	ACC-001-001
36" SMB to BNC male cable - 4 pack	ACC-001-003
6" SMB to BNC female cable	ACC-001-011
6" SMB to BNC female cable - 4 pack	ACC-001-013
6" SMB to SMB jumper cable	ACC-001-021
6" SMB to SMB jumper cable - 4 pack	ACC-001-023
eXpert™ Firmware Options	
eXpert Signal Averaging Firmware Option	250-181-001
eXpert FIR Filtering Firmware Option	250-181-002
eXpert Peak Detection Firmware Option	250-181-003
eXpert Firmware Option bundle (Signal Averaging, FIR Filtering and Peak Detection)	888-100-026

GageScope® Software

GageScope: Lite Edition	Included
GageScope: Standard Edition (with Purchase of CompuScope Hardware)	300-100-351
GageScope: Professional Edition (with Purchase of CompuScope Hardware)	300-100-354

Software Development Kits (SDKs)

GaGe SDK Pack on CD	200-113-000
CompuScope SDK for C/C#	200-200-101
CompuScope SDK for MATLAB	200-200-102
CompuScope SDK for LabVIEW	200-200-103

Updated September 7, 2006

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SMA (M/F) DC to 18 GHz, 2 Watt

Features

- Flat Frequency Response
- Low VSWR
- 2 Watt Rating
- Designed to Meet Environmental Requirements of MIL-A-3933
- Precision Stainless Steel SMA Connectors

Models

- 4779-1, 4779-2, 4779-3, 4779-4, 4779-5, 4779-6, 4779-7, 4779-8, 4779-9, 4779-10, 4779-11, 4779-12, 4779-13, 4779-14, 4779-15, 4779-16, 4779-17, 4779-18, 4779-19, 4779-20, 4779-30, 4779-40, 4779-50, 4779-60

Model	4779-1	4779-2	4779-3	4779-4	4779-5
Low Frequency (GHz)	DC	DC	DC	DC	DC
High Frequency (GHz)	18.0	18.0	18.0	18.0	18.0
Attenuation dB (Nominal)	1	2	3	4	5
Attenuation dB (Deviation DC-12.4)	+/- 0.3	+/- 0.3	+/- 0.3	+/- 0.3	+/- 0.3
Attenuation dB (Deviation 12.4-18)	+/- 0.4	+/- 0.4	+/- 0.3	+/- 0.3	+/- 0.3
Power Input (Max Avg.) in W	2	2	2	2	2
Power Input (Max Peak) in kW	0.2	0.2	0.2	0.2	0.2
VSWR (max) DC-4 GHz	1.15	1.15	1.15	1.15	1.15
VSWR (max) 4-12.4 GHz	1.30	1.30	1.30	1.30	1.30
Maximum Weight (gr)	14	14	14	14	14
Maximum Weight (oz)	0.5	0.5	0.5	0.5	0.5
Special Notes:	A , B , C	A , B , C	A , B	A , B , C	A , B , C

Special Notes:
A: Temperature Coefficient: 0.0006 dB/dB/°C; Power Coefficient: 0.0005 dB/dB/watt.
B: Ordering information: Specify model number and add dash number suffix for attenuation in dB. For example: 4772-10.
C: Standard attenuation values are typically available from stock in the following attenuation values: 3 dB, 6 dB, 10 dB, 20 dB, 30 db. Non-standard attenuation values are available on a custom order basis. Minimum order quantity may apply. Consult factory for details.

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SMA (M/F) DC to 18 GHz, 2 Watt

Model	4779-6	4779-7	4779-8	4779-9	4779-10
Low Frequency (GHz)	DC	DC	DC	DC	DC
High Frequency (GHz)	18.0	18.0	18.0	18.0	18.0
Attenuation dB (Nominal)	6	7	8	9	10
Attenuation dB (Deviation DC-12.4)	+/- 0.3	+/- 0.4	+/- 0.4	+/- 0.4	+/- 0.3
Attenuation dB (Deviation 12.4-18)	+/- 0.3	+/- 0.5	+/- 0.5	+/- 0.5	+/- 0.5
Power Input (Max Avg.) in W	2	2	2	2	2
Power Input (Max Peak) in kW	0.2	0.2	0.2	0.2	0.2
VSWR (max) DC-4 GHz	1.15	1.15	1.15	1.15	1.15
VSWR (max) 4-12.4 GHz	1.30	1.30	1.30	1.30	1.30
Maximum Weight (gr)	14	14	14	14	14
Maximum Weight (oz)	0.5	0.5	0.5	0.5	0.5
Special Notes:	A , B	A , B , C	A , B , C	A , B , C	A , B

Special Notes:
A: Temperature Coefficient: 0.0006 dB/dB/°C; Power Coefficient: 0.0005 dB/dB/watt.
B: Ordering information: Specify model number and add dash number suffix for attenuation in dB. For example: 4772-10.
C: Standard attenuation values are typically available from stock in the following attenuation values: 3 dB, 6 dB, 10 dB, 20 dB, 30 db. Non-standard attenuation values are available on a custom order basis. Minimum order quantity may apply. Consult factory for details.

Model	4779-11	4779-12	4779-13	4779-14	4779-15
Low Frequency (GHz)	DC	DC	DC	DC	DC
High Frequency (GHz)	18.0	18.0	18.0	18.0	18.0
Attenuation dB (Nominal)	11	12	13	14	15
Attenuation dB (Deviation DC-12.4)	+/- 0.5	+/- 0.5	+/- 0.5	+/- 0.5	+/- 0.5
Attenuation dB (Deviation 12.4-18)	+/- 0.6	+/- 0.6	+/- 0.6	+/- 0.6	+/- 0.6
Power Input (Max Avg.) in W	2	2	2	2	2
Power Input (Max Peak) in kW	0.2	0.2	0.2	0.2	0.2
VSWR (max) DC-4 GHz	1.15	1.15	1.15	1.15	1.15
VSWR (max) 4-12.4 GHz	1.30	1.30	1.30	1.30	1.30
Maximum Weight (gr)	14	14	14	14	14
Maximum Weight (oz)	0.5	0.5	0.5	0.5	0.5
Special Notes:	A , B , C	A , B , C	A , B , C	A , B , C	A , B , C

Special Notes:
A: Temperature Coefficient: 0.0006 dB/dB/°C; Power Coefficient: 0.0005 dB/dB/watt.
B: Ordering information: Specify model number and add dash number suffix for attenuation in dB. For example: 4772-10.
C: Standard attenuation values are typically available from stock in the following attenuation values: 3 dB, 6 dB, 10 dB, 20 dB, 30 db. Non-standard attenuation values are available on a custom order basis. Minimum order quantity may apply. Consult factory for details.

SMA (M/F) DC to 18 GHz, 2 Watt

Model	4779-16	4779-17	4779-18	4779-19	4779-20
Low Frequency (GHz)	DC	DC	DC	DC	DC
High Frequency (GHz)	18.0	18.0	18.0	18.0	18.0
Attenuation dB (Nominal)	16	17	18	19	20
Attenuation dB (Deviation DC-12.4)	+/- 0.5	+/- 0.5	+/- 0.5	+/- 0.5	+/- 0.5
Attenuation dB (Deviation 12.4-18)	+/- 0.6	+/- 0.6	+/- 0.6	+/- 0.6	+/- 0.6
Power Input (Max Avg.) in W	2	2	2	2	2
Power Input (Max Peak) in kW	0.2	0.2	0.2	0.2	0.2
VSWR (max) DC-4 GHz	1.15	1.15	1.15	1.15	1.15
VSWR (max) 4-12.4 GHz	1.30	1.30	1.30	1.30	1.30
Maximum Weight (gr)	14	14	14	14	14
Maximum Weight (oz)	0.5	0.5	0.5	0.5	0.5
Special Notes:	A , B , C	A , B , C	A , B , C	A , B , C	A , B

Special Notes:
A: Temperature Coefficient: 0.0006 dB/dB/°C; Power Coefficient: 0.0005 dB/dB/watt.
B: Ordering information: Specify model number and add dash number suffix for attenuation in dB. For example: 4772-10.
C: Standard attenuation values are typically available from stock in the following attenuation values: 3 dB, 6 dB, 10 dB, 20 dB, 30 db. Non-standard attenuation values are available on a custom order basis. Minimum order quantity may apply. Consult factory for details.

Model	4779-30	4779-40	4779-50	4779-60
Low Frequency (GHz)	DC	DC	DC	DC
High Frequency (GHz)	18.0	18.0	18.0	18.0
Attenuation dB (Nominal)	30	40	50	60
Attenuation dB (Deviation DC-12.4)	+/- 0.8	+/- 1.2	+/- 1.2	+/- 1.2
Attenuation dB (Deviation 12.4-18)	+/- 1.0	+/- 1.5	+/- 1.5	+/- 1.5
Power Input (Max Avg.) in W	2	2	2	2
Power Input (Max Peak) in kW	0.2	0.2	0.2	0.2
VSWR (max) DC-4 GHz	1.15	1.15	1.15	1.15
VSWR (max) 4-12.4 GHz	1.35	1.35	1.35	1.35
Maximum Weight (gr)	14	14	14	14
Maximum Weight (oz)	0.5	0.5	0.5	0.5
Special Notes:	A , B	A , B	A , B	A , B

Special Notes:
A: Temperature Coefficient: 0.0006 dB/dB/°C; Power Coefficient: 0.0005 dB/dB/watt.
B: Ordering information: Specify model number and add dash number suffix for attenuation in dB. For example: 4772-10.
C: Standard attenuation values are typically available from stock in the following attenuation values: 3 dB, 6 dB, 10 dB, 20 dB, 30 db. Non-standard attenuation values are available on a custom order basis. Minimum order quantity may apply. Consult factory for details.

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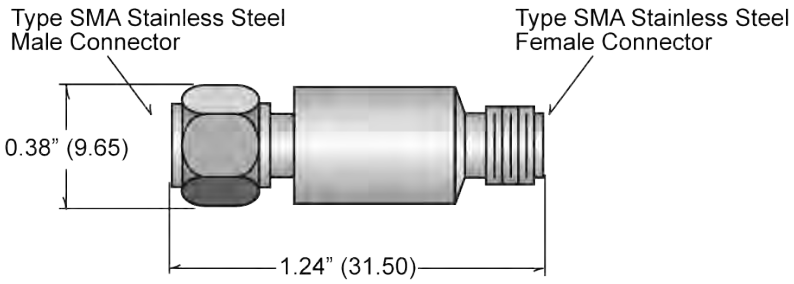
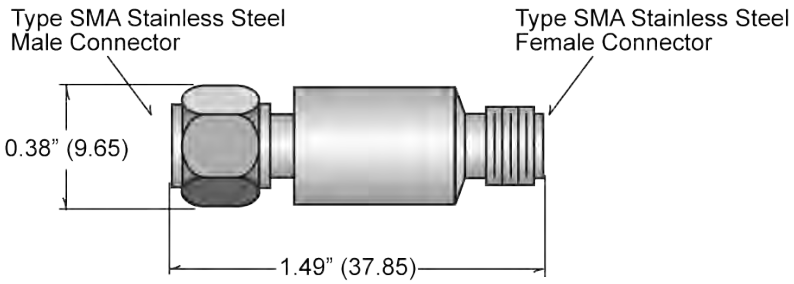
SMA (M/F) DC to 18 GHz, 2 Watt



Outline Drawing for Models:
4779-1, 4779-2, 4779-3, 4779-4, 4779-5, 4779-6, 4779-7, 4779-8, 4779-9, 4779-10, 4779-11, 4779-12, 4779-13, 4779-14, 4779-15, 4779-16, 4779-17, 4779-18, 4779-19, 4779-20, 4779-30

Notes:
Unless otherwise specified dimensions are max. and for reference only. Contact the factory for detailed specifications and outline drawing.



Outline Drawing for Models:
4779-40, 4779-50, 4779-60

Notes:
Unless otherwise specified dimensions are max. and for reference only. Contact the factory for detailed specifications and outline drawing.

Digital Step Attenuator 50Ω DC-4000 MHz

15.5 dB, 0.5 dB Step, 5 Bit, Parallel Control Interface
Single Supply Voltage

ZX76-15R5-PP+

Product Features
- Low Insertion Loss
- High IP3, +52 dBm Typ
- Excellent return loss, 20 dB Typ
- Excellent accuracy, 0.1 dB Typ
- Single Supply Voltage: +3V
- Control inputs buffered by Schmitt Triggers
- Rigid unibody case
- Protected by US patent 6,790,049

Typical Applications
- Lab
- Instrumentation
- Test equipment

CASE STYLE: HK1172

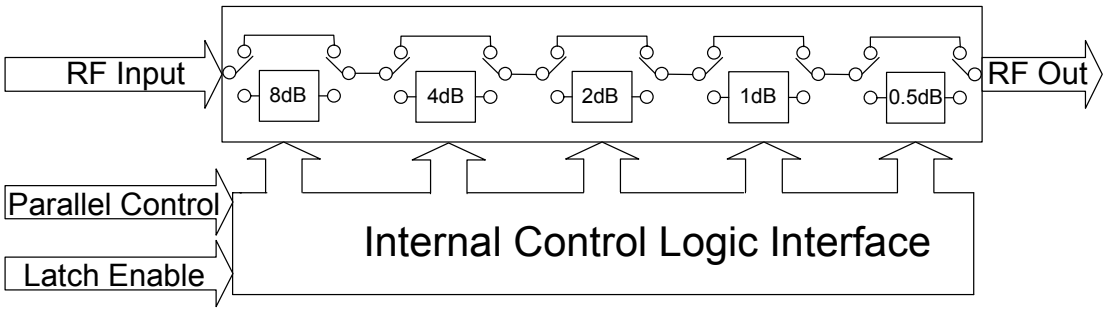
Connectors	Order P/N	Price	Qty.
SMA	ZX76-15R5-PP-S+	$73.95 ea.	(1-9)

+ RoHS compliant in accordance with EU Directive (2002/95/EC)

The +Suffix has been added in order to identify RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

General Description
The ZX76-15R5-PP+ is a 50Ω RF digital step attenuator that offers an attenuation range up to 15.5 dB in 0.5 dB steps. The control is a 5-bit parallel interface. The model operates on a single +3 volt supply. See application note AN-70-004 for 5V supply voltage. The ZX76-15R5-PP+ is produced using a unique case package for ruggedness and operation in tough environments.

Simplified Schematic



RF Electrical Specifications, DC-4000 MHz, T_{AMB}=25°C, V_{DD}=+3V

Parameter	Freq. Range (GHz)	Min.	Typ.	Max.	Units
Accuracy @ **0.5 dB** Attenuation Setting	DC-1	—	0.03	0.1	dB
	1-2.2	—	0.05	0.15	dB
	2.2-4.0	—	0.1	0.35	dB
Accuracy @ **1 dB** Attenuation Setting	DC-1	—	0.02	0.1	dB
	1-2.2	—	0.05	0.15	dB
	2.2-4.0	—	0.1	0.35	dB
Accuracy @ **2 dB** Attenuation Setting	DC-1	—	0.05	0.15	dB
	1-2.2	—	0.15	0.25	dB
	2.2-4.0	—	0.2	0.6	dB
Accuracy @ **4 dB** Attenuation Setting	DC-1	—	0.07	0.2	dB
	1-2.2	—	0.15	0.25	dB
	2.2-4.0	—	0.18	0.6	dB
Accuracy @ **8 dB** Attenuation Setting	DC-1	—	0.03	0.2	dB
	1-2.2	—	0.15	0.3	dB
	2.2-4.0	—	0.5	0.6	dB
Insertion Loss @ all attenuator set to 0dB	DC-1	—	1.5	2.0	dB
	1-2.2	—	1.8	2.5	dB
	2.2-4.0	—	3.0	4.5	dB
IP3 Input * (at Min. and Max. Attenuation)	DC-2.2	—	+52	—	dBm
	2.2-4.0	—	+42	—	dBm
Input Power @ 0.2dB Compression* (at Min. and Max. Attenuation)	DC-4.0	—	+24	—	dBm
VSWR	DC-1	—	1.2	1.5	—
	1-2.2	—	1.2	1.5	—
	2.2-4.0	—	1.8	2.1	—

* IP3 and 1dB compression degrade below 1 MHz

DC Electrical Specifications

Parameter	Min.	Typ.	Max.	Units
V_{DD}, Supply Voltage	2.7	3	3.3	V
I_{DD}, Supply Current	—	—	3	mA
Control Input Voltage Low	0	—	0.3xV_{DD}	V
Control Input Voltage High	0.7xV_{DD}	—	5V	V
Control Current	—	—	400	µA

Switching Specifications

Parameter	Min.	Typ.	Max.	Units
Switching Speed, 50% Control to 0.5dB of Attenuation Value	—	1.0	—	µSec
Switching Control Frequency	—	—	25	kHz

Absolute Maximum Ratings

Parameter	Ratings
Operating Temperature	-40°C to 85°C
Storage Temperature	-40°C to 85°C
V_{DD}	-0.3V Min., 4V Max.
Voltage on Control Input	-0.3V Min., 6V Max.
ESD, HBM	500V
ESD, MM	100V
Input Power	+24dBm

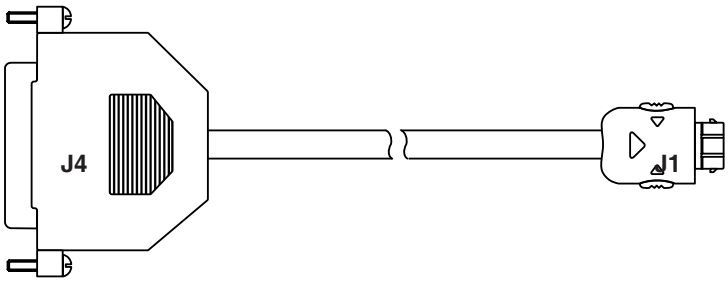
Permanent damage may occur if any of these limits are exceeded

Notes: 1. Performance and quality attributes and conditions not expressly stated in this specification sheet are intended to be excluded and do not form a part of this specification sheet. **2.** Electrical specifications and performance data contained herein are based on Mini-Circuit's applicable established test performance criteria and measurement instructions. **3.** The parts covered by this specification sheet are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp.

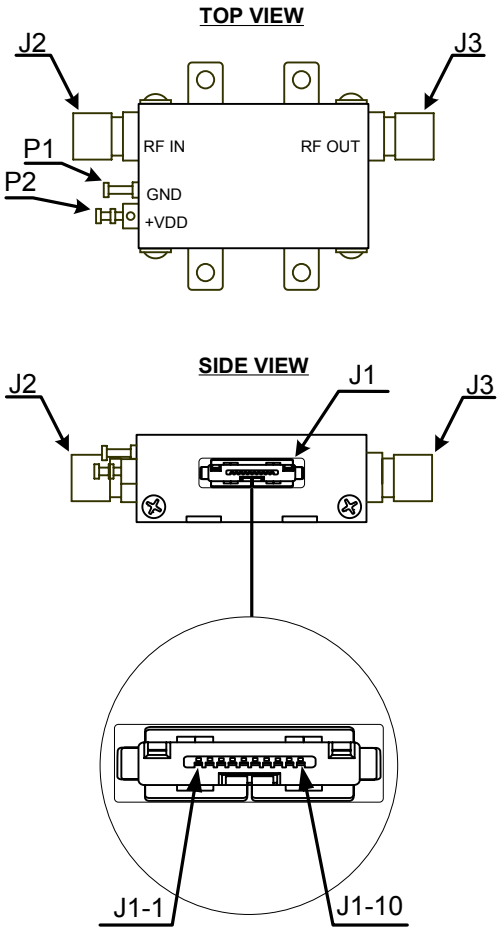
Pin Description

Function	Pin Number	Description
LE	J1-1	Latch Enable Input
C1	J1-2	Control for attenuation bit, 1 dB
C0.5	J1-3	Control for attenuation bit, 0.5 dB
N/C	J1-4	Not Connected
-	J1-5	Not used
GND	J1-6	Ground connection
GND	J1-7	Ground connection
C4	J1-8	Control for attenuation bit, 4 dB
C8	J1-9	Control for attenuation bit, 8 dB
C2	J1-10	Control for attenuation bit, 2 dB
RF in	J2	RF in port (Note 1)
RF out	J3	RF out port (Note 1)
GND	P1	Ground connection
V_{DD}	P2	Positive Supply Voltage

Note 1: Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.



Pin Configuration



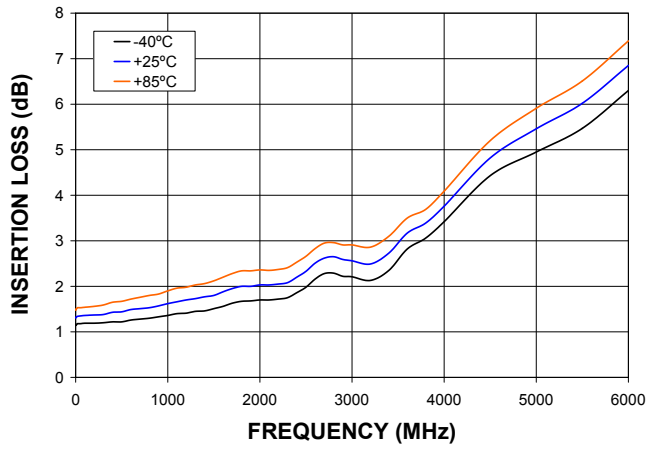
Cable Pin Description

J1-Pin Number	J4-Pin Number	Function	Description	Wire Color
J1-1	J4-8	LE	Latch Enable Input	WHITE
J1-2	J4-3	C1	Control for attenuation bit, 1 dB	YELLOW
J1-3	J4-2	C0.5	Control for attenuation bit, 0.5 dB	GREEN
J1-5	J4-7	-	Not used	BLUE
J1-6	J4-20	GND	Ground connection	BLACK
J1-8	J4-5	C4	Control for attenuation bit, 4 dB	ORANGE
J1-9	J4-6	C8	Control for attenuation bit, 8 dB	BROWN
J1-10	J4-4	C2	Control for attenuation bit, 2 dB	RED

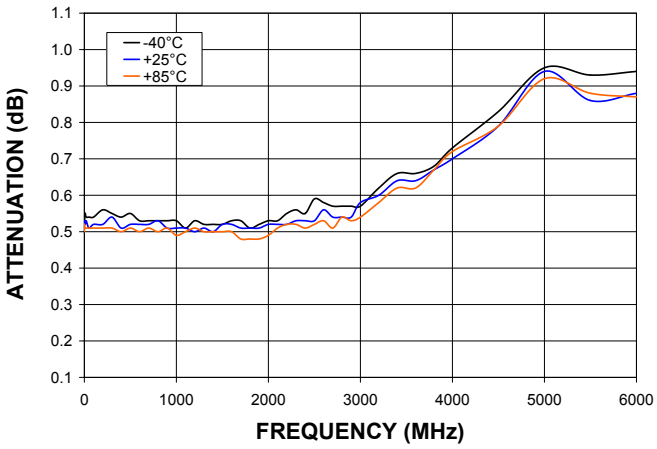
Note: Other pins not connected. Cable shield connected to case ground.

Typical Performance Curves

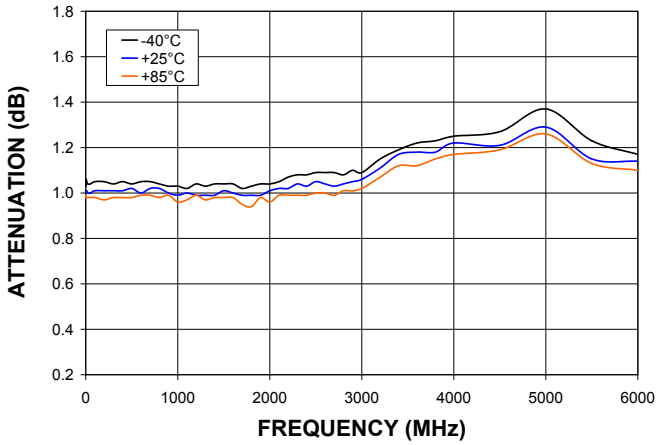
INSERTION LOSS (Ref)



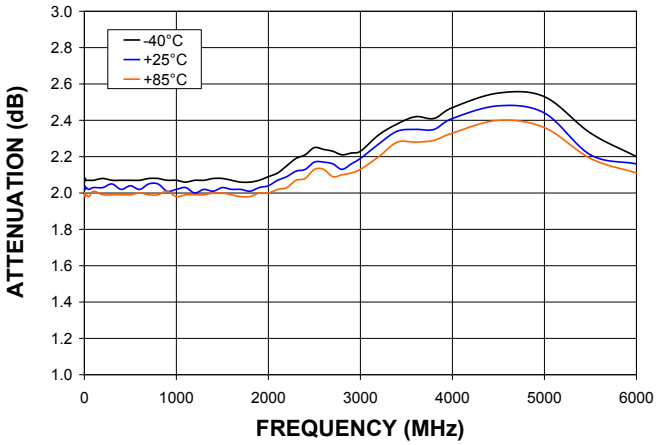
ATTENUATION (0.5 dB)



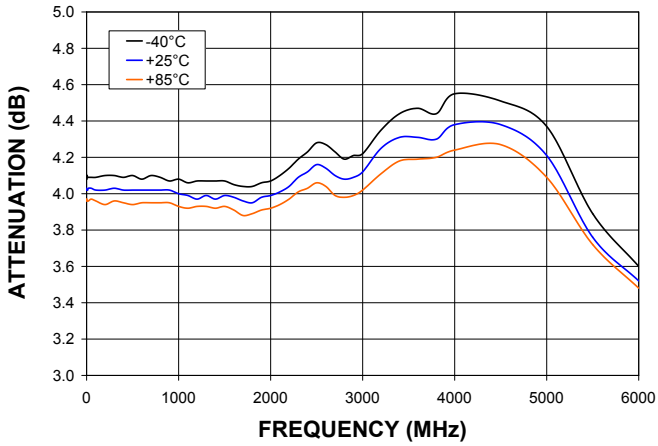
ATTENUATION (1 dB)



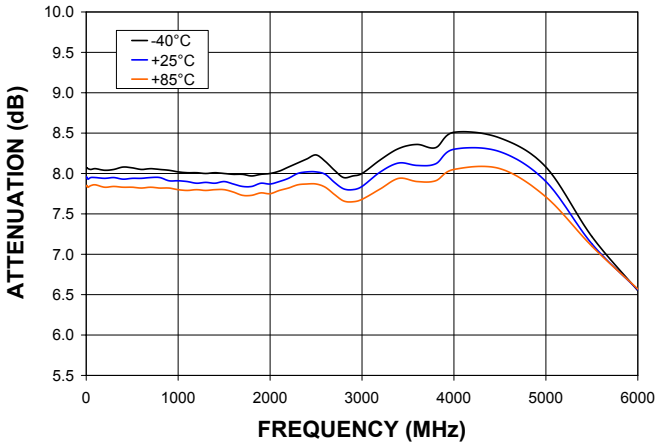
ATTENUATION (2 dB)



ATTENUATION (4 dB)

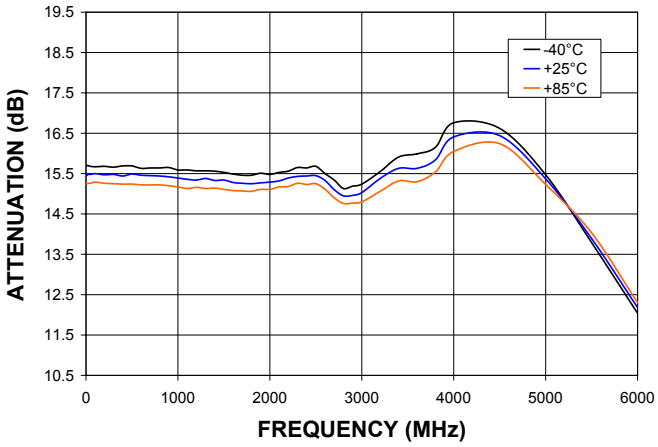


ATTENUATION (8 dB)

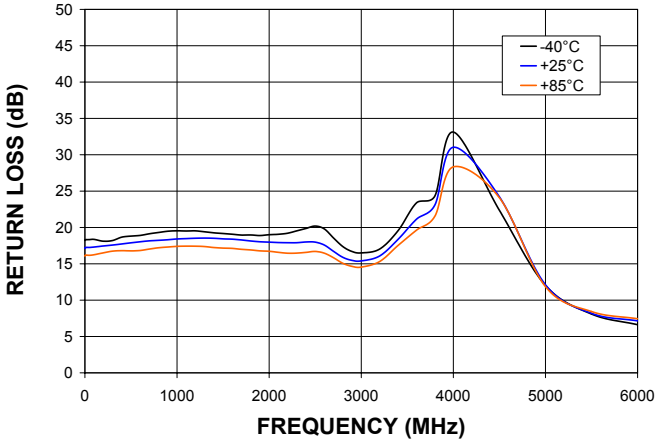


Typical Performance Curves

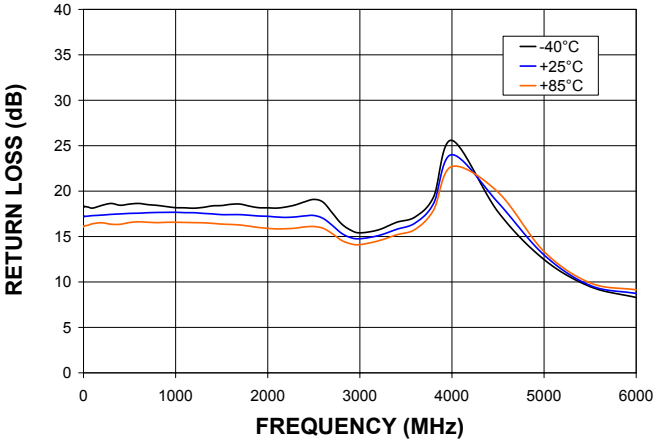
ATTENUATION (15.5 dB)



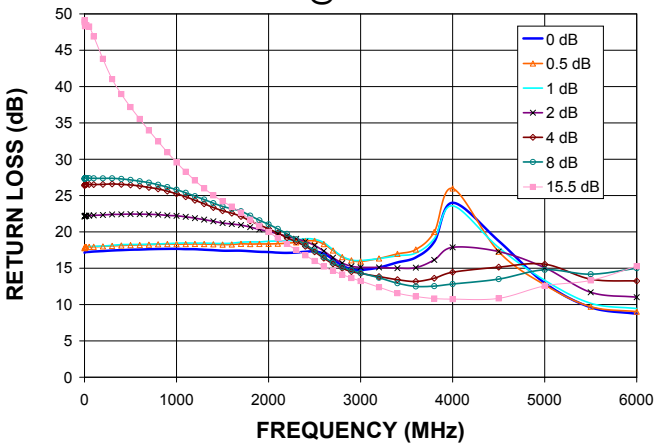
RETURN LOSS IN (Ref)



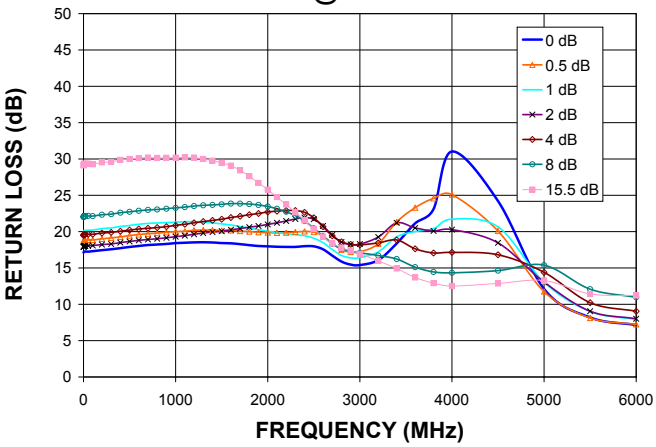
RETURN LOSS OUT (Ref)



RETURN LOSS OUT (Major Atten. Steps) @ +25°C

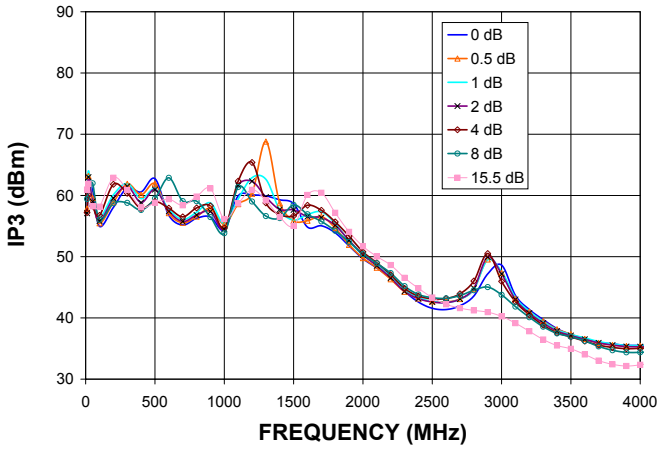


RETURN LOSS IN (Major Atten. Steps) @ +25°C

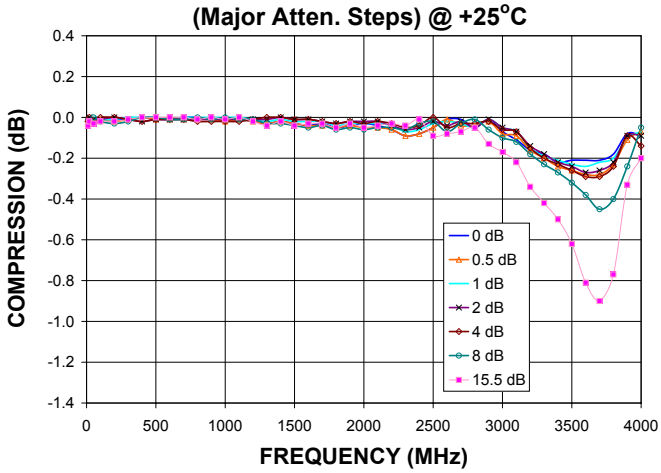


Typical Performance Curves

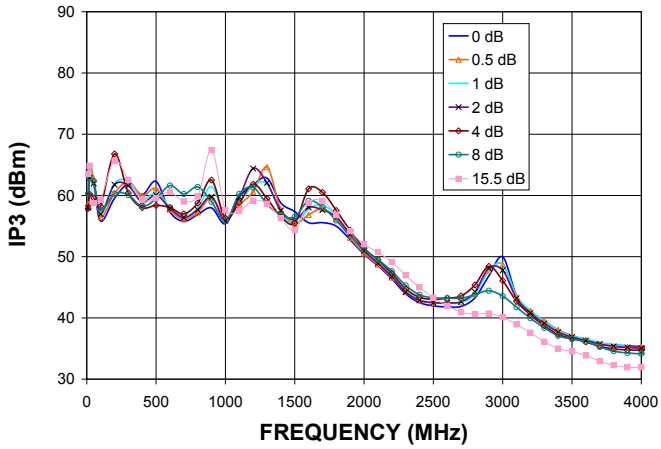
IP3 (Major Atten. Steps) @ +25°C



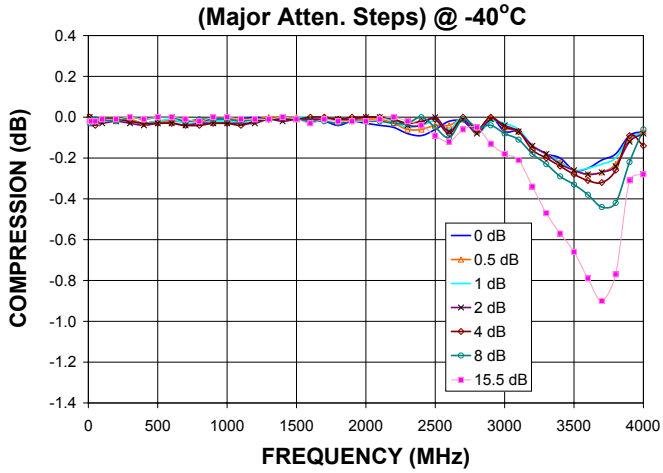
COMPRESSION @ INPUT POWER=+24dBm
(Major Atten. Steps) @ +25°C



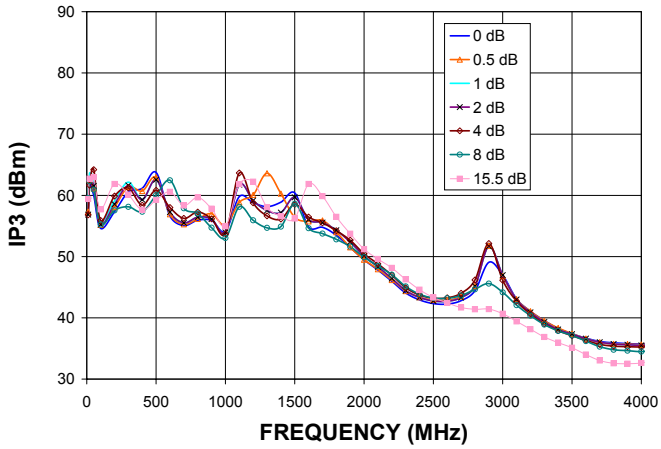
IP3 (Major Atten. Steps) @ -40°C



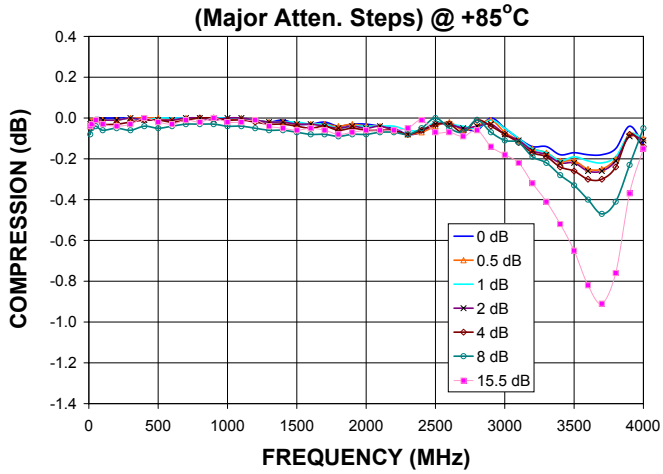
COMPRESSION @ INPUT POWER=+24dBm
(Major Atten. Steps) @ -40°C



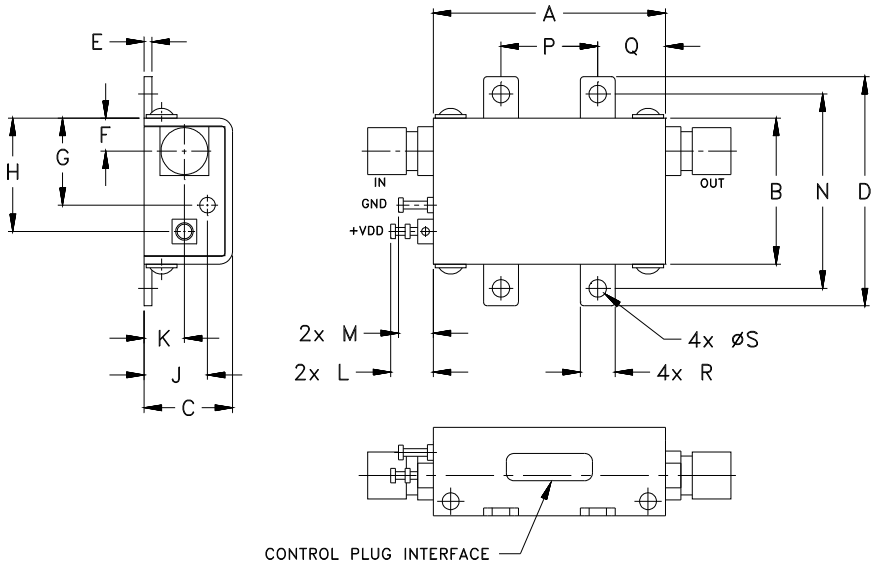
IP3 (Major Atten. Steps) @ +85°C



COMPRESSION @ INPUT POWER=+24dBm
(Major Atten. Steps) @ +85°C



Outline Drawing



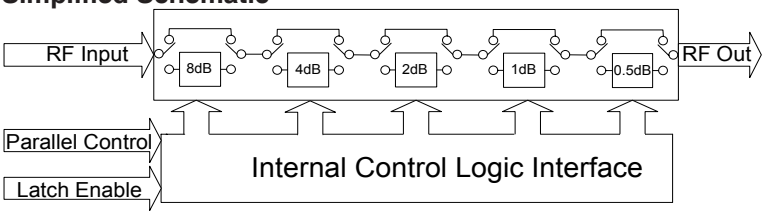
Outline Dimensions (inch/mm)

A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	WT. GRAMS
1.20	**.75**	**.46**	**1.18**	**.04**	**.17**	**.45**	**.59**	**.33**	**.21**	**.22**	**.18**	**1.00**	**.50**	**.35**	**.18**	**.106**	35
30.5	19.1	11.6	30.0	1.0	4.3	11.4	14.9	8.3	5.3	5.6	4.6	25.4	12.7	8.9	4.6	2.69	

Recommended Mounting Hardware:

Use UNC#2 pan head screws with internal tooth lock washers for unit mounting.

Simplified Schematic



The ZX76-15R5-PP+ parallel interface consists of 5 control bits that select the desired attenuation state, as shown in Table 1: Truth Table

Table 1. Truth Table

Attenuation State	C8	C4	C2	C1	C0.5
Reference	0	0	0	0	0
0.5 (dB)	0	0	0	0	1
1 (dB)	0	0	0	1	0
2 (dB)	0	0	1	0	0
4 (dB)	0	1	0	0	0
8 (dB)	1	0	0	0	0
15.5 (dB)	1	1	1	1	1

Note: Not all 32 possible combinations of C0.5 - C8 are shown in table

The parallel interface timing requirements are defined by Figure 1 (Parallel Interface Timing Diagram) and Table 2 (Parallel Interface AC Characteristics), and switching speed.

For latched parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per Figure 1) to latch new attenuation state into device.

For direct parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Control cables for programming and CD with software can be ordered separately. For details see page 9.

Figure 1: Parallel Interface Timing Diagram

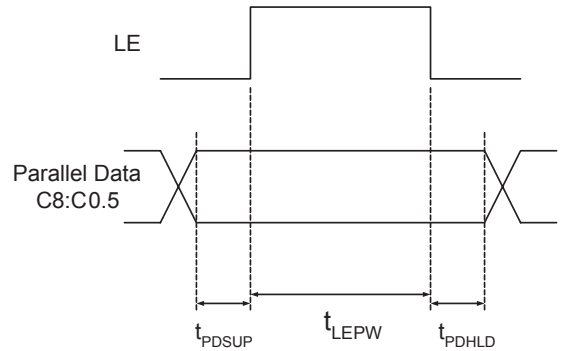


Table 2. Parallel Interface AC Characteristics

Symbol	Parameter	Min.	Units
t_{LEPW}	LE minimum pulse width	10	ns
t_{PDSUP}	Data set-up time before clock rising edge of LE	10	ns
t_{PDHLD}	Data hold time after clock falling edge of LE	10	ns

Power-up State

When the attenuator powers up and LE is logic low, the nominal attenuation is set on 0 dB. When LE is logic high, the nominal attenuation selected upon control logics (see Table 1).

Recommended Accessories

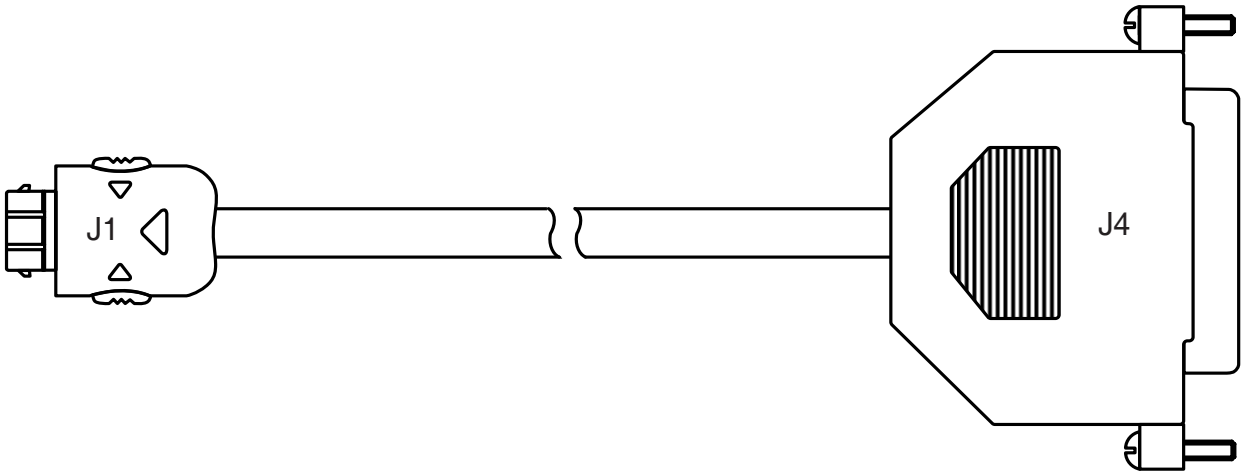
Two optional cable accessories with and without interface connector are available with ZX76-15R5-PP+, the ZX76-CP+ and ZX76-WP+.

ZX76-CP+ shielded cable with interface 25 pin D-type connector and supplied software are used to control the ZX76-15R5-PP+ digital attenuator from a computer, using LPT port.

ZX76-WP+ shielded cable without interface 25 pin D-type connector enables customer to use the ZX76-15R5-PP+ digital attenuator in his own application. Cable length is 4.9 feet / 1.5 meters.

Note: Mini-Circuits can supply control cables with other options for the J4 connector and/or different cable lengths. Consult factory with your specific requirements.

ZX76-CP+ Control Cable

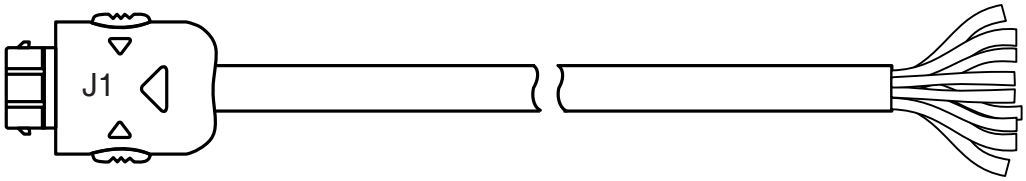


ZX76-CP+ wiring information

J1-Pin Number	J4-Pin Number	Function	Description	Wire Color
J1-1	J4-8	LE	Latch Enable Input	WHITE
J1-2	J4-3	C1	Control for attenuation bit, 1 dB	YELLOW
J1-3	J4-2	C0.5	Control for attenuation bit, 0.5 dB	GREEN
J1-5	J4-7	-	Not used	BLUE
J1-6	J4-20	GND	Ground connection	BLACK
J1-8	J4-5	C4	Control for attenuation bit, 4 dB	ORANGE
J1-9	J4-6	C8	Control for attenuation bit, 8 dB	BROWN
J1-10	J4-4	C2	Control for attenuation bit, 2 dB	RED

Note: Other pins not connected. Cable shield connected to case ground.

ZX76-WP+ Control Cable



ZX76-WP+ wiring information

Pin Number	Function	Description	Wire Color
J1-1	LE	Latch Enable Input	WHITE
J1-2	C1	Control for attenuation bit, 1 dB	YELLOW
J1-3	C0.5	Control for attenuation bit, 0.5 dB	GREEN
J1-5	-	Not used	BLUE
J1-6	GND	Ground connection	BLACK
J1-8	C4	Control for attenuation bit, 4 dB	ORANGE
J1-9	C8	Control for attenuation bit, 8 dB	BROWN
J1-10	C2	Control for attenuation bit, 2 dB	RED

Note: Other pins not connected. Cable shield connected to case ground.

Ordering Information

Model Number	Description	Quantity Min. No. of Units	Price $ Ea.
ZX76-15R5-PP-S+	Digital attenuator - Parallel interface Single Positive Supply Voltage	1-9	73.95
ZX76-CP+	Cable accessory with interface connector	1	24.95
ZX76-WP+	Cable accessory without interface connector	1	22.95
ZX76-CD*	CD ROM ZX76 programming software	1	No Charge

*Note: To receive the CD, request when placing order.

5 Volt-Surface Mount

Monolithic Amplifier

DC-7 GHz

Product Features

- High Gain, 24 dB typ. at 100 MHz
- High Pout, P1dB 20.5 dBm typ. at 100 MHz
- High IP3, 37 dBm typ. at 100 MHz
- Ruggedized design
- Fixed 5V operation
- Unconditionally stable
- Excellent ESD Protection
- Transient protected, US patent 6,943,629

Typical Applications

- Base station infrastructure
- Portable Wireless
- CATV & DBS
- MMDS & Wireless LAN
- LTE

GVA-84+

CASE STYLE: DF782
PRICE: $1.82 ea. QTY. (30)

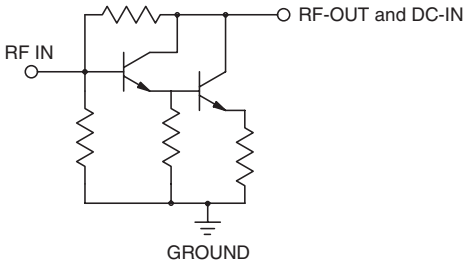
+ RoHS compliant in accordance with EU Directive (2002/95/EC)

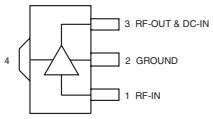
The +Suffix has been added in order to identify RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

General Description

GVA-84+ (RoHS compliant) is a wideband amplifier offering high dynamic range. Lead finish is SnAgNi. It has repeatable performance from lot to lot and is enclosed in a SOT-89 package. It uses patented Transient Protected Darlington configuration and is fabricated using InGaP HBT technology.

simplified schematic and pin description





Function	Pin Number	Description
RF IN	1	RF input pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation.
RF-OUT and DC-IN	3	RF output and bias pin. DC voltage is present on this pin; therefore a DC blocking capacitor is necessary for proper operation. An RF choke is needed to feed DC bias without loss of RF signal due to the bias connection, as shown in "Recommended Application Circuit", Fig. 2
GND	2,4	Connections to ground. Use via holes as shown in "Suggested Layout for PCB Design" to reduce ground path inductance for best performance.

Electrical Specifications[1] at 25°C and 5V, unless noted

Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range[2]		DC		7	GHz
Gain	0.1	22.9	24.1	25.3	dB
	1.0		21.7		
	2.0	17.4	18.4	19.9	
	3.0		16.0		
	4.0	13.8	14.6	16.3	
	6.0		12.5		
	7.0		10.5		
Magnitude of Gain Variation versus Temperature[3] (values are negative)	0.1		0.0004		dB/°C
	1.0		0.0021		
	2.0		0.0032	0.006	
	3.0		0.0044		
	4.0		0.0058		
	6.0		0.0131		
	7.0		0.0175		
Input Return Loss	0.1		22.9		dB
	1.0		20.6		
	2.0	15.0	18.5		
	3.0		18.1		
	4.0		19.1		
	6.0		17.9		
	7.0		11.9		
Output Return Loss	0.1		23.3		dB
	1.0		10.7		
	2.0	6.0	7.7		
	3.0		7.1		
	4.0		7.0		
	6.0		6.3		
	7.0		5.6		
Reverse Isolation	2.0		26.5		dB
Output Power @1 dB compression	0.1	19.4	20.4		dBm
	1.0	19.5	20.5		
	2.0	19.6	20.6		
	3.0		21.0		
	4.0		19.9		
	6.0		17.0		
	7.0		15.6		
Saturated Output Power (at 3dB compression)	0.1		21.7		dBm
	1.0		22.3		
	2.0		22.3		
	3.0		22.2		
	4.0		21.0		
	6.0		18.9		
	7.0		17.2		
Output IP3	0.1	33.0	36.7		dBm
	1.0	32.2	35.8		
	2.0	32.9	36.6		
	3.0		35.8		
	4.0		34.9		
	6.0		33.0		
	7.0		32.0		
Noise Figure	0.1		5.5	6.5	dB
	1.0		5.6		
	2.0		5.5	6.5	
	3.0		5.5		
	4.0		5.6	6.6	
	6.0		6.2		
	7.0		6.8		
Group Delay	2.0		94		psec
Device Operating Voltage		4.8	5.0	5.2	V
Device Operating Current		85	108	130	mA
Device Current Variation vs. Temperature			61.8		µA/°C
Device Current Variation vs Voltage			0.058		mA/mV
Thermal Resistance, junction-to-ground lead			64		°C/W

[1] Measured on Mini-Circuits test board TB-313. See Characterization Test Circuit (Fig. 1)
[2] Guaranteed specification DC-7 GHz. Low frequency cut off determined by external coupling capacitors and external bias choke.
[3] (Gain at 85°C - Gain at -45°C)/130

Absolute Maximum Ratings

Parameter	Ratings
Operating Temperature (ground lead)	-45°C to 85°C
Storage Temperature	-65°C to 150°C
Operating Current at 5V	160mA
Power Dissipation	1W
Input Power	13 dBm
DC Voltage on Pin 3	5.8V

Note:
Permanent damage may occur if any of these limits are exceeded.
Electrical maximum ratings are not intended for continuous normal operation.

Characterization Test Circuit

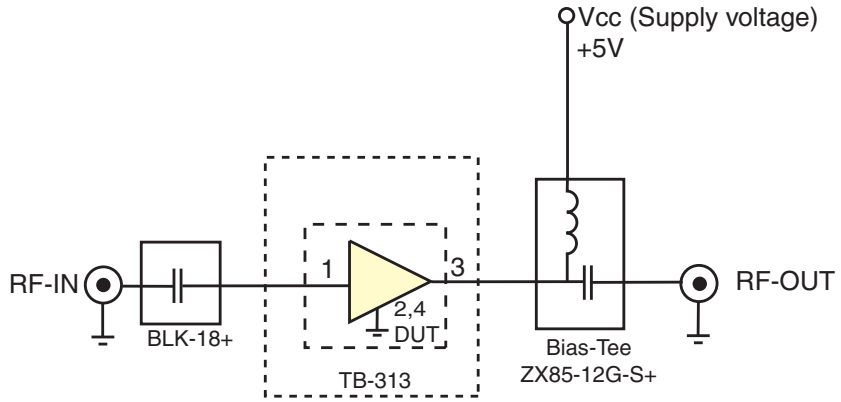
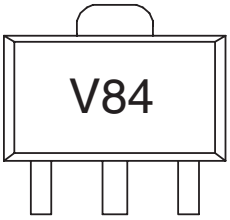


Fig 1. Block Diagram of Test Circuit used for characterization. (DUT soldered on Mini-Circuits Test Board TB-313)

Gain, Output power at 1dB compression (P1 dB) and output IP3 (OIP3) are measured using R&S Network Analyzer ZVA-24. Noise Figure measured using Agilent's N5242A PNA-X microwave network analyzer.

Conditions:
1. Gain and Return loss: Pin= -25dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 0 dBm/tone at output.

Product Marking



Additional Detailed Technical Information

Additional information is available on our web site. To access this information enter the model number on our web site home page.

Performance data, graphs, s-parameter (S2P FILES) data set (.zip file)

Case Style: DF782 (SOT 89)
Plastic package, exposed paddle, lead finish: tin/silver/nickel

Tape & Reel: F55

Suggested Layout for PCB Design: PL-255

Evaluation Board: TB-410-84+

Environmental Ratings: ENV08T2

Recommended Application Circuit

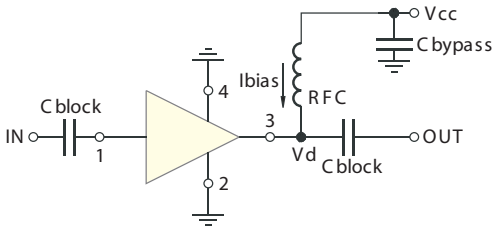


Fig 2. Test Board includes case, connectors, and components soldered to PCB

ESD Rating

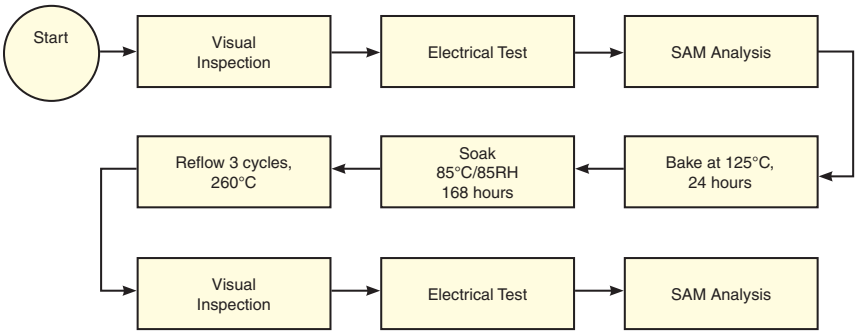
Human Body Model (HBM): Class 1C (1000v to < 2000v) in accordance with ANSI/ESD STM 5.1 - 2001

Machine Model (MM): Class M2 (100V to < 200V) in accordance with ANSI/ESD STM 5.2 - 1999

MSL Rating

Moisture Sensitivity: MSL1 in accordance with IPC/JEDECJ-STD-020C

MSL Test Flow Chart



Coaxial

Power Splitter/Combiner

ZAPD-4+

2 Way-0° 50Ω 2000 to 4200 MHz

N-Type version shown

CASE STYLE: F14

Connectors	Model	Price	Qty.
N-TYPE	ZAPD-4-N+	$64.95	(1-9)
SMA	ZAPD-4-S+	$64.95	(1-9)

+ RoHS compliant in accordance with EU Directive (2002/95/EC)

The +Suffix has been added in order to identify RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

Maximum Ratings

Operating Temperature	-55°C to 100°C
Storage Temperature	-55°C to 100°C
Power Input (as a splitter)	10W max.
Internal Dissipation	0.125W max.

Permanent damage may occur if any of these limits are exceeded.

Coaxial Connections

SUM PORT	S
PORT 1	1
PORT 2	2

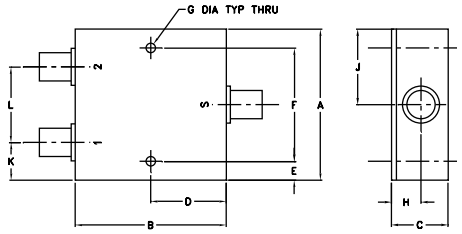
Features

- wideband, 2000 to 4200 MHz
- low insertion loss, 0.4 dB typ.
- good isolation, 25 dB typ.
- up to 10W power input as splitter
- excellent amplitude unbalance, 0.1 dB typ.
- excellent phase unbalance, 0.5 deg. typ.
- rugged shielded case

Applications

- MMDS
- ISM
- wireless
- communication systems
- instrumentation

Outline Drawing



Outline Dimensions (inch / mm)

A	B	C	D	E	F	G
2.00	2.00	0.75	1.00	0.25	1.500	0.125
50.80	50.80	19.05	25.40	6.35	38.10	3.18

H	J	K	L	wt
0.39	1.00	0.50	1.00	grams
9.91	25.40	12.70	25.40	170.0

Electrical Specifications

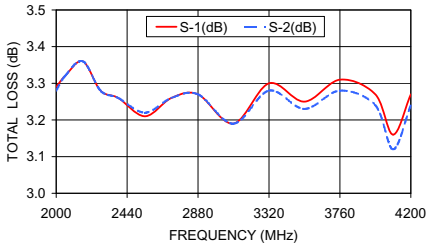
FREQ. RANGE (MHz)	ISOLATION (dB)		INSERTION LOSS (dB) ABOVE 3.0 dB		PHASE UNBALANCE (Degrees)	AMPLITUDE UNBALANCE (dB)
f_L-f_U	Typ.	Min	Typ.	Max.	Max.	Max.
2000-4200	25	19	0.4	0.8	6	0.4

Typical Performance Data

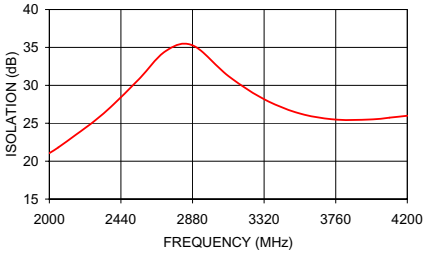
Frequency (MHz)	Total Loss[1] (dB)		Amplitude Unbalance (dB)	Isolation (dB)	Phase Unbalance (deg.)	VSWR S	VSWR 1	VSWR 2
	S-1	S-2						
2000.00	3.29	3.28	0.01	21.06	0.12	1.33	1.10	1.10
2055.00	3.32	3.32	0.00	21.81	0.06	1.32	1.11	1.11
2165.00	3.36	3.36	0.00	23.52	0.02	1.28	1.12	1.12
2275.00	3.28	3.28	0.01	25.26	0.06	1.26	1.12	1.13
2385.00	3.26	3.26	0.01	27.29	0.06	1.25	1.14	1.16
2550.00	3.21	3.22	0.01	30.80	0.03	1.23	1.16	1.19
2715.00	3.26	3.26	0.00	34.52	0.07	1.22	1.15	1.20
2880.00	3.27	3.27	0.01	35.28	0.11	1.24	1.19	1.25
3100.00	3.19	3.19	0.01	31.23	0.05	1.23	1.20	1.27
3320.00	3.30	3.28	0.02	28.17	0.13	1.25	1.22	1.28
3540.00	3.25	3.23	0.02	26.28	0.06	1.20	1.21	1.26
3760.00	3.31	3.28	0.02	25.49	0.06	1.16	1.15	1.20
3980.00	3.27	3.24	0.04	25.51	0.02	1.10	1.13	1.17
4090.00	3.16	3.12	0.03	25.74	0.04	1.09	1.10	1.15
4200.00	3.27	3.24	0.04	25.99	0.02	1.10	1.08	1.13

1. Total Loss = Insertion Loss + 3dB splitter loss.

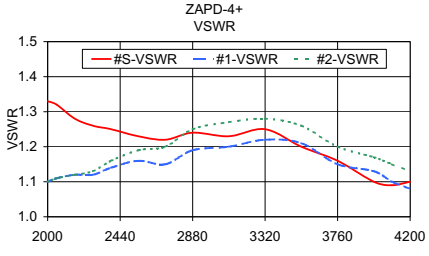
ZAPD-4+
TOTAL LOSS



ZAPD-4+
ISOLATION



ZAPD-4+
VSWR



electrical schematic

REV. C
M127604
ZAPD-4+
HY/TD/CP/AM
100614

FEATURES AND APPLICATION:

180° hybrid adopts strip line structure, it gets low insertion loss, high isolation, good amplitude and phase accuracy, and high power handling.

Broad band 180° hybrid is mainly used for EW, radar fields, combining power, discovering and tracking signal, single pulse radar and antenna and feeder system.

TECHNICAL SPECIFICATIONS:

Frequency Range	Insertion Loss	Isolation	VSWR	Amplitude Balance
2-4GHz	0.60dB	20dB	1.60	±0.5dB

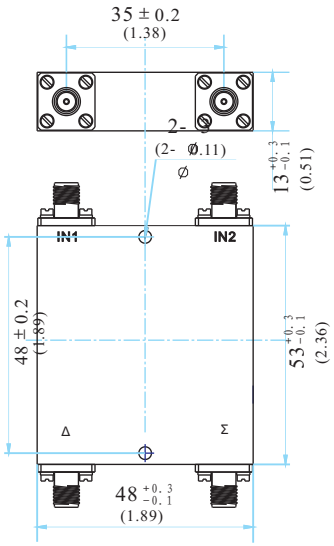
Phase Balance	Connector	Power Handling
±10°	SMA-F	50W

ENVIRONMENTAL PARAMETERS:

WORKING TEMPERATURE: -55~+85℃

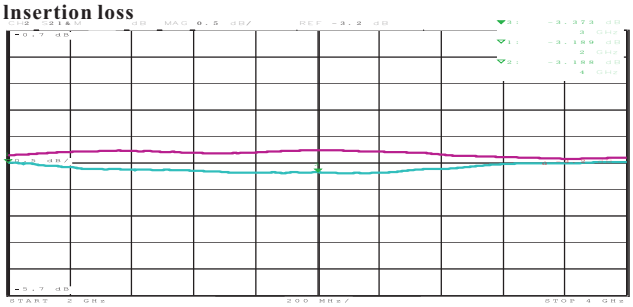
STORAGE TEMPERATURE: -55~+100℃

OUTLINE: mm (inch)

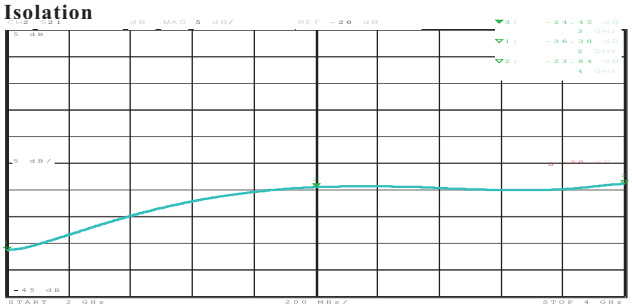


TYPICAL PLOT:

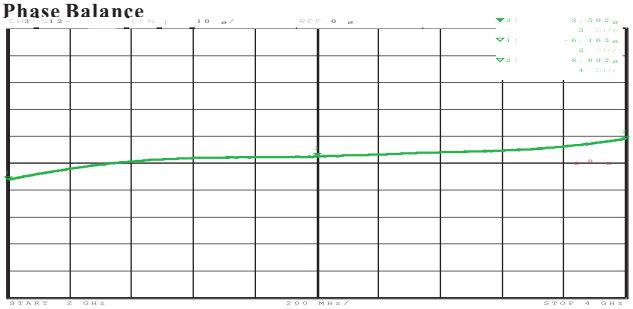
Insertion loss



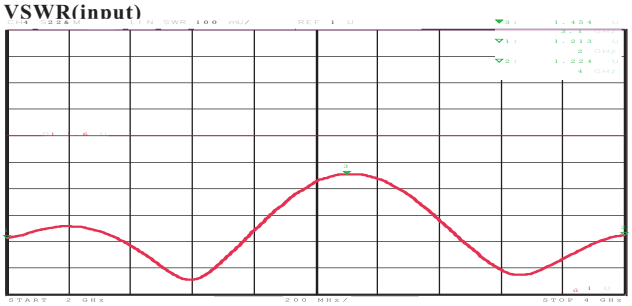
Isolation



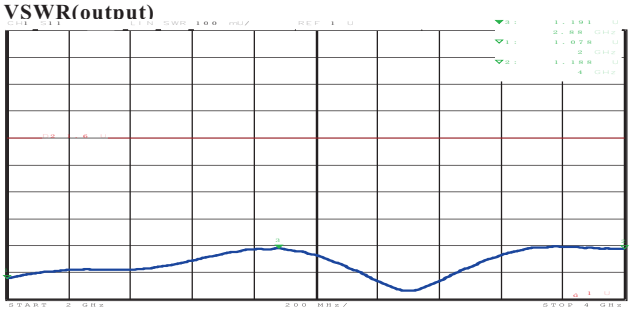
Phase Balance



VSWR(input)



VSWR(output)



SW-475

SPDT High Isolation Terminated Switch
0.5 - 3.0 GHz

Rev. V6

Features

- Positive Voltage Control (0 / +5 V)
- High Isolation (53 dB typ. @ 0.9 GHz, 50 dB typ @ 1.9 GHz)
- 50-Ohm Internal Terminations
- Low Insertion Loss (0.6 dB typ. @ 0.9 GHz, 0.7 dB typ. @ 1.9 GHz)
- 4 mm 16-Lead PQFN Package

Description

The M/A-COM SW-475 GaAs monolithic switch provides high isolation in a low-cost, plastic surface mount package. The SW-475 is ideal for applications across a broad range of frequencies including synthesizer switching, transmit / receive switching, switch matrices and filter banks in systems such as radio and cellular equipment, PCS, GPS, and fiber optic modules.

M/A-COM fabricates the SW-475 using a 1.0-micron gate length MESFET process. The process features full chip passivation for performance and reliability.

Ordering Information [1]

Part Number	Package
SW-475 PIN	Bulk Packaging
SW-475TR	1000 piece reel
SW-475TR-3000	3000 piece reel
SW-475SMB	Sample board

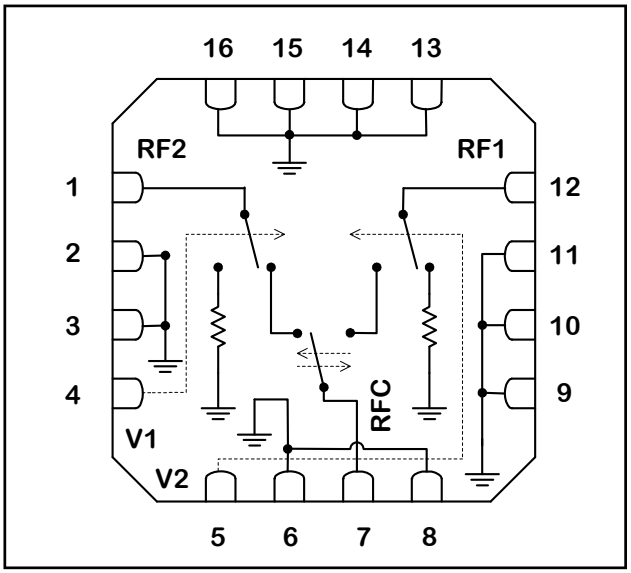
1. Reference Application Note M513 for reel size information.

Absolute Maximum Ratings [2]

Parameter	Absolute Maximum
Input Power (0.5 - 3.0 GHz)	
3 V Control	+30 dBm
5 V Control	+33 dBm
Operating Voltage	+8.5 volts
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

2. Exceeding any one or combination of these limits may cause permanent damage to this device.

Functional Schematic



PIN Configuration

Pin	Function	Description
1	RF2	RF port
2	GND	RF ground
3	GND	RF ground
4	V1	Control 1
5	V2	Control 2
6	GND	RF ground
7	RFC	RF port
8	GND	RF ground
9	GND	RF ground
10	GND	RF ground
11	GND	RF ground
12	RF1	RF port
13	GND	RF ground
14	GND	RF ground
15	GND	RF ground
16	GND	RF ground
17 (pad)[3]	GND	RF ground

3. The exposed pad centered on the package bottom must be connected to RF and DC ground.

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• **India** Tel: +91.80.43537383 • **China** Tel: +86.21.2407.1588
Visit www.macomtech.com for additional data sheets and product information.

Electrical Specifications [4]: T_A = 25 °C, V_{CTL} = 0, 5.0 V (unless otherwise specified)

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	0.5- 1 GHz 1.0 - 2.0 GHz 2.0 - 3.0 GHz	dB dB dB	— — —	0.6 0.7 0.75	0.7 0.8 0.9
Isolation	0.5 - 1 GHz 1.0 - 2.0 GHz 2.0 - 3.0 GHz	dB dB dB	51 48 45	54 52 50	— — —
Return Loss	0.5 - 1 GHz 1.0 - 2.0 GHz 2.0 - 3.0 GHz	dB dB dB	15 15 15	20 20 20	— — —
Input IP_2	2-Tone 900 MHz, 5 MHz spacing (V_C = 5.0 V)	dBm	—	83	—
Input IP_3	2-Tone 900 MHz, 5 MHz spacing (V_C = 5.0 V)	dBm	—	46	—
P1dB	1 GHz, 5 V 1 GHz, 3 V	dBm dBm	— —	27 18	— —
P0.1dB	1 GHz, 5 V 1 GHz, 3 V	dBm dBm	— —	24 11	— —
T_{RISE}, T_{FALL}	10% to 90% RF & 90% to 10% RF	nS	—	24	—
T_{ON}, T_{OFF}	50% of V_C to 10 % / 90% RF	nS	—	15	—
Transients	V_C = 5.0 V square wave, in-band	mV	—	12	—
Control Current	|Vc| = 4.5 V, 0 dBm	µA	—	2	13

4. DC blocking capacitors requires on all RF ports.

Truth Table [5]

V1	V2	RFC - RF1	RFC - RF2
0	1	ON	OFF
1	0	OFF	ON

5. External DC blocking capacitors required on all RF ports. We recommend 47 pF.

Logic Level	Voltage Level
0	0 V ± 0.2 V
1	3.0 V to 8.0 V

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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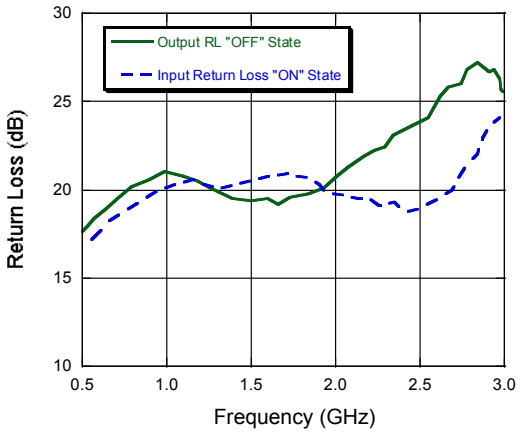
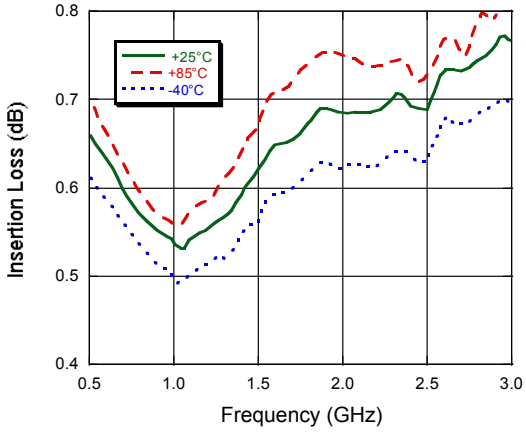
Typical Performance Curves

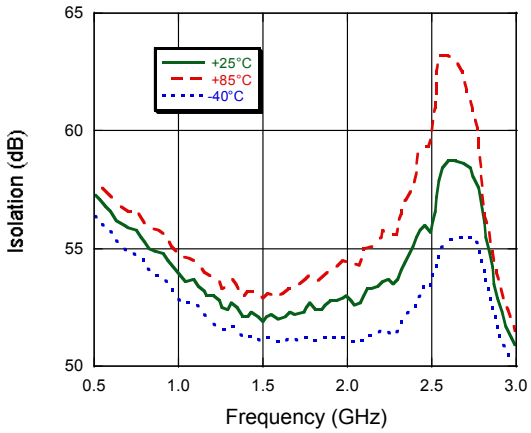
Return Loss Vs. Frequency



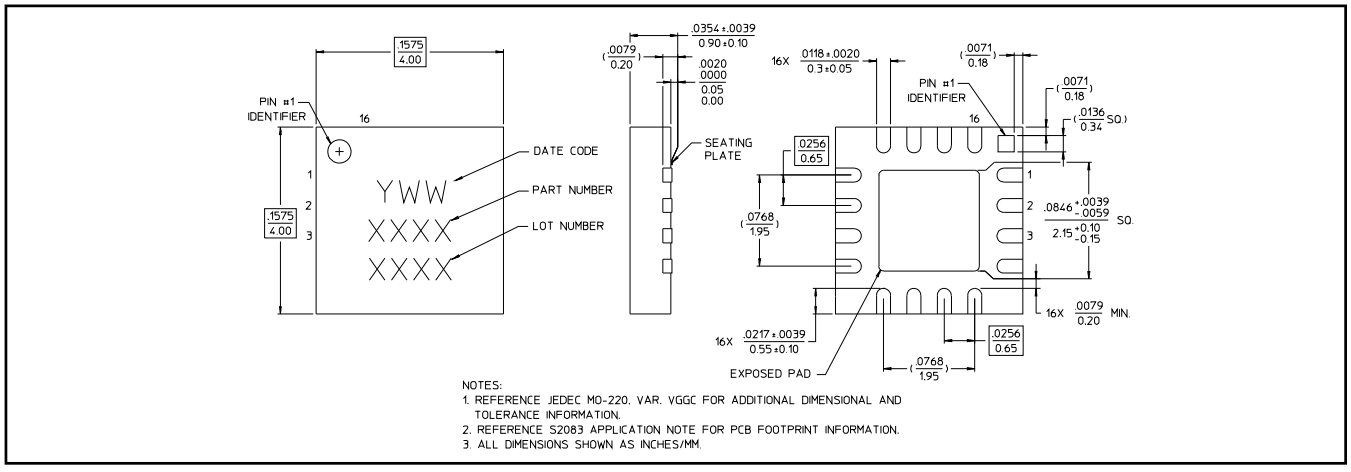
Insertion Loss Vs. Temperature



Isolation Vs. Frequency Over Temperature



4 mm 16-Lead PQFN



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